boundary surface area is reduced. This lowers the energy of the film through elimination of the energy associated with grain boundaries. This normal grain growth occurs till the grain size is slightly larger than or equal to the film thickness and a columnar structure develops. At this point it is empirically observed that normal grain growth stops [11]. However, if the temperature of annealing is raised, grain growth can occur through secondary grain growth (after normal grain growth has stopped). It has been observed that secondary grains often have restricted or uniform crystallographic texture [25]. In case of p-doped polysilicon secondary grains have (111) texture [11, 25].

In films that are thinner than the average grain size, the top and the bottom surfaces can play very important roles in the selective growth of secondary grains. The driving force (ΔF_s) for growth of a secondary grain, which is due to the fact that the surface energy of the crystal, is a function of its orientation. can be given by [26]

$$\Delta F_s = \frac{2(\gamma - \gamma_s)}{h} \qquad (6.2)$$

where γ is the average surface energy of the normal grains, γ_s is the surface energy of the secondary grain, and h is the film thickness. Those grains that have orientations, which lead to low surface energies, have the highest driving force for growth as secondary grains. This accounts for the texture development during the thin film secondary grain growth.

Once a secondary grain begins to grow, it grows at a rate given by [26]

$$\dot{r}_s \propto \left(\frac{2\Delta\gamma}{h}\right) \qquad (6.3)$$

where $\Delta\gamma = \gamma - \gamma_s$. It should be noted that in equations (6.2) and (6.3) it is implicitly assumed that the top and bottom surfaces are identical. If this were not true, different values of $\Delta\gamma$ would apply at each surface. Secondary grain growth is highest in thinner

films as illustrated in equation (6.3). The final secondary grain size, however, is a function of the number of properly oriented grains in the initial normal grain structure.

Thompson and Smith [11] have reported observing secondary grain growth in 75-nm thick films with phosphorus doping, yielding grains up to 40 times the films thickness when annealed at 1300 °C. The activation energy of this process was reported to be 3.8 eV. Secondary grain growth has also been reported after rapid-thermal annealing of phosphorus-doped films at temperatures in excess of 1000 °C [12]. We observed this effect (secondary grain growth) in the case of polysilicon films annealed at 1000 °C to grow gate oxide during transistor fabrication (Section 4.3.2). This process does realize significantly larger grains but the disadvantage is the fairly high temperature required.

6.3 TECHNIQUES TO CONTROL GRAIN BOUNDARY LOCATION

Controlling the grain boundary location such that the device region is free of them can also reduce the detrimental effect of grain boundaries on the device characteristics. This can be achieved by selectively seeding nuclei in the precursor amorphous films and fabricating devices in the laterally crystallized regions around the seeded region. This seeding can be done in several ways. The key to this process is ensuring that the deposition conditions of the precursor amorphous films are adjusted so that no spontaneous nucleation occurs in the films during the lateral crystal growth. In the following sections we will describe these methods in some detail.

6.3.1 Lateral solid phase epitaxy over oxide

The most obvious source for nucleation seed is the Si substrate itself. The advantage is that the grain orientation is also controlled by the orientation of the Si substrate and single-crystal Si on insulator can be obtained. The process involves patterning of SiO_2 to create holes such that the *a*-Si layer, deposited later, is in intimate

contact with the Si substrate. Within these holes, vertical solid phase epitaxial (SPE) occurs on heating provided the interface between *a*-Si and the Si substrate is free of contaminants. Prolonged heating will result in the outward growth of the initially formed single crystal region and this epitaxial expansion of the seed region into the amorphous Si film over the adjoining SiO_2 will continue until the nucleation and growth of randomly oriented crystallites eventually consumes the remaining *a*-Si. This phenomenon is termed as lateral solid phase epitaxy (LSPE). The final condition of the sample consists of single crystal portions aligned with the substrate and polycrystalline region covering most of the oxide [27, 28].

The key issue is the extent of epitaxial propagation away from the initial seed, and this depends on several factors, the most important being the rate of SPE relative to random crystallization in the amorphous films. The competition between the two processes is a strong function of temperature as they have different activation energies as we discussed earlier, and hence lower annealing temperatures are preferred. It also depends on the crystallographic orientation of the seed as the SPE rates is a strong function of crystal orientation, with the <100>-oriented growth front have a growth rate about 25 times that of the <111>-oriented growth front [29]. The random nucleation rate in the *a*-Si can be also be suppressed relative to the SPE rates by increasing the disorder in the *a*-Si films as discussed in Section 6.2.1. The predicted propagation distances for LSPE of Si at temperatures below 650 °C (~10 μm) with *a*-Si deposited by LPCVD are adequate to permit the fabrication of devices and circuits [27].

The extent of LSPE also depends on the orientation of the edges of the oxide openings. It was found that random crystallization rate was accelerated at the edges of the patterned oxide compared to regions far away from the edges. This might be due to the stress caused by the differential thermal expansion [27]. Ishiwara and Yamamoto [28]

have found that the rate of LSPE is less than the rate of vertical SPE for the same film, implying that some type of Si/SiO_2 interface interaction occurs, which inhibits the lateral movement of the crystal/amorphous boundary. Ishiwara et al [28] have also proposed that the ~5-10 % decrease in specific volume that occurs during crystallization of *a*-Si might create stresses at the growth interface leading to enhanced random nucleation of crystallites in the adjoining *a*-Si film.

Low-temperature LSPE offers great promise to realize SOI films and is adaptable for use in fabrication of three-dimensional, multilayer integrated circuits. In fact, Subramanian et al [30] have recently reported on the use of LSPE from the etched Si vertical sidewalls to form ultrathin-channel SOI sub-100 nm transistors. They implanted Si at a dose of $5x10^{15}$ cm^{-2} after the *a*-Si deposition to destroy the native oxide at the interface of the *a*-Si/single crystal Si to grow single-crystal Si laterally over the underlying oxide. However, the extension of LSPE is still not quite that much to have complete flexibility in the fabrication of 3-D ICs. This technique also needs an underlying Si substrate as the seed, and is therefore not suitable for display applications.

6.3.2 Selective-nucleation-based epitaxy

This technique does not strictly involve solid phase crystallization. It involves direct deposition of crystalline silicon in which nucleation sites are manipulated by modifying the amorphous surface. This technique has been termed as selective-nucleation-based epitaxy (sentaxy) [31] and is based on the concept of graphoepitaxy [32], where the crystallographic orientation of thin films is controlled by micro-patterning the underlying amorphous substrate surface (will be discussed later in section 6.5.1).

Thin film growth on amorphous substrate involves nucleation, growth and coalescence. Nucleation and growth are affected by adsorption rate, surface diffusion rate and desorption rate and these depend strongly on the substrate surface material as

well as the growth conditions. In addition, the chemical reaction of the adatoms with the surface material is a dominant factor in determining the growth mechanisms. Sentaxy involves patterning small regions on which nucleation takes place readily (Si_3N_4) over a substrate surface, which has an extremely low nucleation density (SiO_2). When the deposition starts on the surface-modified substrates, only one nucleus is formed (to ensure this, the nucleation density is controlled by careful addition of HCl during growth) on the Si_3N_4 region that is an artificial-nucleation site. The periodically located nuclei increase in size eventually grow over the substrate surface and impinge on adjacent growing islands which nucleated from other sites. This method thereby enables one to manipulate the nucleation sites and grow large single-crystal islands at predetermined locations.

The growth was carried out at substrate temperature of ~1000 °C using $SiCl_4$ and H_2. The silicon islands grew up to 100 μm (using 1.2-μm diameter Si_3N_4 islands on SiO_2) in size and had highly faceted surface, which is typical of direct-deposited crystalline Si. The Si films had strong (110) texture. P-channel transistors made in the films after planarizing had field-effect mobility of 180 cm^2/Vs, which is comparable to values obtained in bulk silicon [31].

This technique is innovative and does realize single-crystal Si on insulator. However, the method involves high temperature processing and the resulting films are rough requiring costly polishing and lapping before devices can be fabricated in them.

6.3.3 Other selective seeding/lateral crystallization techniques

Other seeding techniques have been tried to control location of grain boundaries. They involve laser crystallization, metal-induced crystallization, germanium-induced crystallization, temperature-gradient-induced lateral crystallization and plasma-induced seeding. We have already described most of these seeding techniques, especially metal

and germanium-seeding techniques earlier in Sections 2.2.3 and 4.5.1, and hydrogen plasma seeding in Section 4.5. However, we will revisit some of the seeding methods and describe them briefly.

Laser-induced nucleation

Toet et al [33] have demonstrated the use of laser crystallization to induce nucleation in selective regions of the amorphous Si films and subsequently annealed them to realize large grains in the laterally crystallized regions around the seeds. This process involved no lithography and the processing temperature was kept below 600 °C. A grid of crystallization seeds was created by locally melting the *a*-Si using cw Ar^+-focused 1-μm laser beam. The films were subsequently annealed at 600 °C and the seeded regions grew radially outwards resulting in star-like domains around the seeded regions. A strain gradient is created around the seed. This stress arises from the increase in the density of the material upon crystallization, combined with differential contraction between laser-crystallized material and the substrate. This strain gradient results in the diffusion of Si atoms towards the seed and thereby enhancing the radial growth rate [34]. These films had grains up to 5 μm in length. No data on the electrical characteristics (TFT data) has yet been reported.

For large area processing laser interference is suggested to create the grid. However, this requires expensive equipment. These films have the usual crystalline defects found in SPC films like microtwins, stacking faults, etc, and therefore the disadvantage of both SPC and laser-induced crystallization apply in this case. Further work is necessary to optimize the process.

Metal or Germanium-induced nucleation

As we have discussed previously, metals like Ni and Pd, and germanium have also been used to seed nucleation in selective regions. In fact Ni and Ge have been used

to seed crystal growth locally in the source/drain regions of the transistor and hence improve the field-effect mobility due to reduced number of grain boundaries in the channel.

The Ni seeding was accomplished by deposition of 2-nm thick Ni layer after the source/drain implantation [35]. Spin coating of Ni solution has also been reported [36]. The crystallization anneal and the implant damage anneal was then simultaneously carried out leading to lateral crystal growth from the source/drain regions into the channel. In the case of Ni, at the early stage of the MIC/MILC heat treatment, Ni readily reacts with *a*-Si and converts itself into $NiSi_2$. Nucleation and growth of crystal grains occur randomly along the interface between the $NiSi_2$ and the underlying *a*-Si. At the edges of the Ni covered region, a few of the $NiSi_2$ nodules break away and move laterally into regions not covered by Ni. As the nodules move laterally, any *a*-Si along its path is crystallized leading to MILC [37]. Ni enhances the grain growth of Si by as much as two orders of magnitude compared to intrinsic Si due to faster diffusion of NiS_2. Due to this the lateral growth can continue for over 100 μm before random nucleation occurs. Transistors showed nearly four times improvement in field-effect electron mobility compared to the unseeded devices. The disadvantage is the residual Ni in the silicon films [35, 38].

Subramanian et al [39] have reported the use of germanium to control grain boundary locations and have used this technique to fabricate TFTs. The germanium was deposited in selective regions of the *a*-Si films through opening in a sacrificial oxide. After the Ge deposition the films were annealed in argon at 500-550 °C to fully crystallize the channel films. The remaining Ge was then removed by wet etching and standard self-aligned top-gate TFTs were fabricated with dry thermal oxide as the gate dielectric (900-°C process). Single seeded (seeded only in the drain) and dual seeded

(seeded in source and drain) devices were compared with the unseeded control devices. As expected the single-seeded devices have the highest electron mobility of ~300 cm^2/Vs compared to ~250 cm^2/Vs for the dual-seeded devices and ~100 cm^2/Vs for the unseeded devices. The field-effect mobility of the seeded TFTs showed a strong dependence on the channel length and width of the devices, with the smallest device showing the maximum mobility. This is because for a small device the laterally crystallized region is a larger portion of the channel. We observed the similar dependence of field-effect mobility on the channel length for the hydrogen-plasma-dual-seeded TFTs (discussed in Section 4.5.4). The drawback of the germanium seeding is the residual germanium contamination in the films.

Lateral crystallization through patterned-light-absorption masks

Thermal gradient during crystallization has also been used to realize lateral crystallization of *a*-Si films [40]. This technique requires transparent substrates and the crystallization is accomplished by rapid thermal annealing using tungsten-halogen lamps. The thermal gradient was established using patterned-light-absorption masks (*a*-Si film) deposited on the surface of the film. Due to increased absorption in the regions with patterned *a*-Si layer a thermal gradient develops, resulting in elongated grains along the thermal gradient. To ensure localized heating, transparent substrates are necessary. This technique resulted in increase in field-effect electron mobility at shorter channel lengths of ~65 for the seeded case vs. ~41 cm^2/Vs for the unseeded case [40]. The advantage of this technique is that there is no extra contamination introduced in the films, unlike the case of germanium or metal seeding. However, the need for transparent substrates limits its applicability.

6.4 TECHNIQUES TO MINIMIZE AND PASSIVATE DEFECTS

In addition to increasing the grain size and controlling the grain boundary locations, there is need for reducing the crystalline defects within the grains and defects at the grain boundaries, so that single-crystal like behavior can be achieved. As mentioned in Section 2.2 earlier, SPC annealed films are characterized by several kinds of crystalline defects like microtwins and stacking faults and the number of defects depends on the deposition conditions of the *a*-Si films, the *a*-Si/substrate interface, the annealing conditions, etc. Several techniques have been tried to minimize these defects.

6.4.1 Techniques to minimize crystalline defects

To achieve single-crystal Si like behavior reduction of the number of defects is essential. These defect/trap states arise at the grain boundaries of the polysilicon films due to the presence of silicon dangling bonds and also due to the presence of crystalline defects like microtwins and stacking faults in the grains. The grain-boundary defects usually have a stronger detrimental effect on the carrier transport characteristics compared to intra-grain defects. Grain-boundary effect can be minimized by grain size enlargement and using selective-seeding techniques to ensure that the grain boundaries are outside the device region as discussed in the previous section. In this section we will concentrate on the techniques used to minimize the intra-grain defects of SPC polysilicon films.

High-temperature anneal

As mentioned earlier, SPC polysilicon films contain large number in-grain defects, mainly microtwins [41] (see Section 2.2). Coherent twins are generally electrically inactive. However, since they terminate inside the crystal they introduce electrically active defects [42], which act as scattering sites, resulting in a smaller effective grain size. Microtwins in polysilicon are unstable, and annealing at

temperatures above 750 °C can drastically reduce their density [41, 43]. Girginoudi et al [44] have used rapid thermal annealing at 850 °C for 30 s for five times after complete crystallization of the *a*-Si film at 600 °C to minimize the number of twinning defects in the film as monitored by the reduction in the electron spin resonance (ESR) signal. This was also confirmed by the increase in the Hall electron mobility of the samples from 26 cm^2/Vs to 43 cm^2/Vs [44] and increase in field-effect electron mobility of TFTs from 25 to 35 cm^2/Vs [43] after the high-temperature anneal.

Laser anneal

Instead of high-temperature anneal, excimer laser annealing after the SPC step can also control the number of twins in the films [45].

Effect of *a*-Si/SiO_2 interface on defect generation

The phase transformation from the amorphous to the crystalline phase is accompanied with an increase in the density and this results in tensile stress in the amorphous matrix surrounding the crystalline regions [24] (also discussed in Section 3.3.5). Crystalline defects (dislocations, twins, etc) develop during the nucleation stage to relieve this stress. This stress is largest at the *a*-Si/SiO_2 interface [24] as the Si atoms in the *a*-Si are strongly bound to the surface atoms of the underlying SiO_2 layer after deposition [46]. As the nucleation predominantly occurs at that interface the (discussed previously in Section 6.2.3) twinning is quite high in typical SPC films. On the other hand, the Si atoms at the surface are only loosely bound to the native SiO_2 layer and the stress generated upon nucleation can easily be relieved thus minimizing the creation of twins. Morimoto et al [24] have demonstrated the formation of a nearly defect-free crystalline Si layer by removing the SiO_2 underlayer before the anneal during lateral SPE from substrate-seeded region. By this technique they could extend the defect-free LSPE region by nearly a factor of two compared to without removing the underlying

SiO_2. Ryu et al [8] have also seen reduction in defects by suppressing interface nucleation due a similar effect (see Section 6.2.3 for further details). In our work, the hydrogen plasma treatment of the *a*-Si:H film results in nucleation at the surface and hence the number of crystalline defects might be lower compared to untreated films that nucleate at the bottom. However, we have not been able to confirm this effect as it is difficult to draw any conclusions from the TEM pictures.

Continuous grain polycrystalline silicon

Recently a new type of silicon film has been developed where the each crystal grain constituting the film has continuity in atomic configuration at the crystal grain boundaries [47-49] . This new material formed by the solid phase crystallization of amorphous silicon by a novel crystallization technique has been named continuous grain silicon (CGS). In CGS, the {111} lattice is continuously connected at the grain boundary, whereas in conventional polysilicon, since the lattice join at random angles, there is misfit of lattice between adjacent grains. Accordingly, the atomic bonds at the boundary are smooth in CGS, whereas numerous dangling bonds exist at the grain boundaries in conventional polysilicon films leading to degradation of carrier mobility. TFTs made in CGS films show excellent properties close to that of single-crystal with field-effect mobility of ~300 cm^2/Vs [47, 49]. This technology has also been applied in liquid crystal panel for 2.6-inch digital TV [48]. This technique has the potential for use in SOI technology too. However, we could find no references describing the process to obtain CGS films in detail.

6.4.2 Passivation of defects

Our real goal is to eliminate defects altogether. But at present there is still need to reduce the effect of trap states (usually at the grain boundaries) on the electronic properties of the polysilicon. For this purpose hydrogenation of the films is typically

carried out. Hydrogenation results in passivation of dangling bonds at the grain boundaries with hydrogen [50, 51]. Hydrogenation of the films is usually accomplished by exposing the films to a hydrogen plasma [51] to generate the hydrogen atoms, which form the Si-H bonds and hence reduce the number of dangling bonds in the layer. The hydrogenation is typically carried out at increased substrate temperature (~300 °C) to enhance the hydrogen diffusion through the bulk of the film. In our work, the fabrication of transistors involved a hydrogenation step as described in Section 4.3. Hydrogenation also played a critical part in the fabrication of integrated amorphous and polycrystalline TFTs described in chapter 5, to passivate the defect states in both the amorphous regions after the high-temperature anneal.

Several other methods of hydrogenation have also been tried: implanting H^+ into the films followed by an anneal at 400 °C for 10 min in N_2 [52], sintering of Al contacts in presence of LPCVD Si_3N_4 encapsulating layer [53] so that the hydrogen generated at the Al-Si contact remains in the films, and hot-wire hydrogenation [54] wherein hydrogen atoms are generated by thermal dissociation of hydrogen gas using a resistively-heated tungsten wire (temperature of 1900 °C). In addition, remote hydrogen plasma treatment [55] has also been used to reduce the plasma damage to the gate dielectric due to charging (discussed in chapter 7) or UV photons during direct plasma exposure.

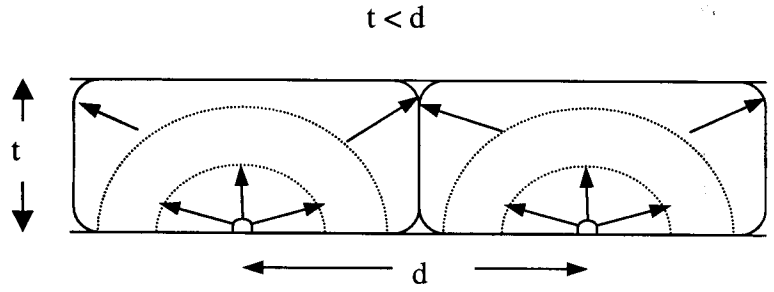
Other passivation techniques, by using O_2 [56], or NH_3 [57]or N_2O [58], and F [59] have also been reported. Oxygen and hydrogen plasma treatment led to the most drastic improvement in the performance of transistors compared to only hydrogen plasma treatment. Chern at al [56, 60] speculated that oxygen atoms passivate the dangling bonds. Similar effect was observed during the ECR plasma oxidation of polysilicon films [61], with the ESR signal intensity (a measure of the dangling bonds density) decreased due to the plasma treatment. However, this conclusion was contested by Nickel et al [62] who

argued that oxygen plasma treatment led to cleaning of the surface and the passivation of dangling bonds was due to hydrogen only, which was generated from water vapor in the chamber during the oxygen plasma treatment. We believe a similar circumstance occurs during the oxygen plasma treatment of *a*-Si:H in our work studying the plasma-enhancement of crystallization of *a*-Si:H films (discussed in Section 3.5). Addition of either argon or N_2 to the hydrogen plasma [51] or using NH_3 plasma [57, 63] increased the hydrogenation efficiency. It is speculated that nitrogen also passivates the dangling bonds, and as the Si-N bonds are stronger than Si-H, the passivation is more efficient than just hydrogenation. This results in improved reliability against hot-carrier degradation [57].

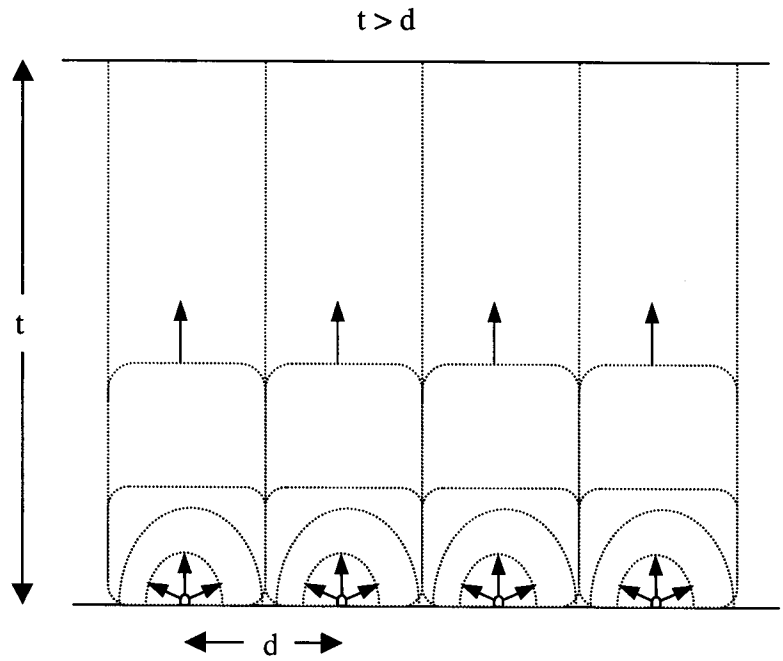
All this work goes to prove that defect passivation plays a very important role in the characteristics of the polysilicon devices.

6.5 GRAIN ORIENTATION

Typically in solid phase crystallized polysilicon films the grains are oriented in the (111) vertical direction as discussed in section 3.3.8. The typical shape of grains in these films is ellipsoidal with two fast growing axes along the [110] and [112] and the slow axis along the [111] direction [64]. The preferential growth of grains along the <112> and <110> directions is due to orientation-dependent growth rates and the fact that growing crystals are bounded by the slowest growing crystallographic facets. In silicon <100> is the fastest growth direction, followed by the <113>, <110>, <112>, and finally the <111>, being 1.5, 3, 5, and 25 times slower, respectively [29, 65]. The difference in the growth rate is related to the number of Si atoms which is incorporated in order to complete a sixfold ring. Thus, for <100> only one Si atom is needed, while for <110> and <111> two and three atoms must be incorporated, respectively, to



(a)



(b)

Figure 6.1. The mode of growth in two extreme cases is presented considering heterogeneous nucleation at the interface. (a) The thickness t of the film is low compared to the mean distance d of the nuclei at the interface; this is a case of low nucleation density. In this case a laminar structure is developed parallel to the substrate. (b) The thickness t of the film is very high compared to the mean distance d of the nuclei at the interface; this is the case of high nucleation density. In this case a columnar structure is developed perpendicular to the substrate [64].

complete a hexar structure. This means facets oriented in the <111> direction bound the growing crystal. The <111>-oriented surface also has the least surface energy [11] and hence is energetically favored as the crystallization occurs due to the free energy gained by the phase transformation and minimization of the surface energy.

As we discussed earlier in Section 6.2.3, nucleation typically occurs at the *a*-Si/SiO_2 substrate interface [6, 22, 66]. For the case of thin films (film thickness t is less than the typical distance d between the nuclei, i.e. the grain size of the film polysilicon), the crystallites grow first in a three-dimensional way and when they reach the surface the growth proceeds in a two-dimensional way (Fig. 6.1(a)) and the resulting structure is laminar [64]. Crystal growth during furnace annealing of thin *a*-Si:H film on glass or SiO_2/Si substrate occurs in this fashion. For the case when t>>d, the crystallites grow in three-dimensional manner as described earlier until they impinge on others, then, the growth continues in one dimension perpendicular to the film/substrate interface (Fig. 6.1(b)). So the structure of the film in this case is columnar [64]. The case of columnar growth can be applied to direct deposition of polysilicon films, as the density of nucleation centers is very high and the growth perpendicular to the substrate is unlimited.

Due to the anisotropic growth rates, in thin films with low density of nucleation centers at the interface, nuclei with orientation permitting a fast growth parallel to the substrate are extended laterally at the expense of other nuclei that do not have this favorable orientation. This lateral growth is only stopped by impingement on an adjacent crystallite. In this case, large crystallite with the <111>-preferred orientation, i.e. the slowest growth direction, perpendicular to the substrate are predominant. This might explain the strong <111> texture of the SPC films. The same effects predominate during growth in surface nucleated films as confirmed by the strong <111> texture in

hydrogen and oxygen plasma-treated films with the only difference being that the growth starts from the surface till it reaches the substrate and then growth proceeds laterally.

6.5.1 Graphoepitaxy

Even though solid phase crystallized polysilicon films are typically oriented in the <111> vertical direction, they are randomly oriented in the plane of the film leading to random bond angles at the grain boundaries. This results in dangling bonds and therefore creation of trap states that degrades performance of devices. There is need therefore to control the in-plane grain orientation of the polysilicon films top to maximize field-effect mobility and achieve single-crystal like behavior. Uniform {100}-oriented (vertical and in-plane) surface have been achieved for laser crystallized and zone-melt recrystallized films with the crystallization starting from the liquid phase [67, 68] using special techniques like either orientation filtering or surface relief grating on the substrate to realize uniform in-plane orientation. These techniques have been termed as artificial epitaxy or graphoepitaxy as it involves oriented growth of crystalline films on amorphous substrates through an artificial or manmade lattice rather than by a crystalline (atomic) lattice, as occurring in classical (atomic) epitaxy.

A theoretical model predicts that, film-formation methods that yield textured polycrystalline films (i.e., the individual crystal grains have one particular plane parallel to the substrate surface and random orientation otherwise) on smooth amorphous substrates should yield uniformly oriented films, if such film formation is carried out over an appropriate surface-relief structure in the amorphous substrate. For example, polysilicon films with (100) texture should become uniformly oriented on a surface-relief grating with square-wave cross-section, if the spatial period of the grating is small compared to the normal grain size. Polysilicon films with (111) texture (obtained after

SPC as mentioned earlier), on the other hand, would require a relief structure having facets that intersect at 70.5° and/or 109.5°. Relief structures with square-wave cross section are more easily fabricated using current techniques, thus one is led to seek polysilicon formation methods that yield (100) or (110)-textured silicon. Under certain conditions laser crystallization [68] and zone-melting recrystallization [69] using a strip heater of *a*-Si is known to yield silicon films with (100) texture. Graphoepitaxy using these two techniques of crystallization have been studied since 1980s [70].

When a Si film on a textured SiO_2 substrate, encapsulated with SiO_2, is heated by irradiation, the Si partially melts for certain range of radiant power density. Solid crystallites are stable in this melt for a fixed radiant power density [71]. These crystallites have (100) texture [72] and have a preferential <100> orientation parallel to the grating axis. These crystallites act as seeds during the subsequent solidification leading to the uniform overall (100) texture of the films [70].

Graphoepitaxy using solid-state grain growth has also been studied [73]. The lynchpin of this technique is the surface-energy-driven growth of secondary grains in thin films at high temperatures (as discussed in Section 6.2.4). Surface-energy-driven grain growth is a solid-state process in which grains that are oriented such that the sum of the free energies of their top and bottom surfaces is a minimum, grow by consuming neighboring grains [11, 32, 74]. This results in grains with uniform texture, though randomly oriented in the in-plane direction. In case of germanium, with both surfaces encapsulated with SiO_2 secondary grain growth yielded grains with a predominant (110) texture and 4-5 μm in diameter [74]. A surface-relief grating in the SiO_2, substrate with 0.2 μm period square-wave profile then resulted in the growth of Ge grains with (100) texture and <100> directions preferentially parallel to the grating axis [73]. For Si,

however, secondary grain growth results in grains with (111) texture [11] and hence the grating profile to control in-plane orientation needed would be saw-toothed. No report of graphoepitaxy using secondary grain growth in silicon films has been found, although the group working on continuous grain silicon (discussed in Section 6.4.1) might have used some kind of textured substrate to control the in-plane grain orientation and hence reduce the number of dangling bonds at the grain boundaries.

6.6 SUMMARY AND FUTURE WORK

To summarize, we have examined the key issues in achieving single-crystal like Si on an insulating substrate by solid-phase crystallization of *a*-Si. We have reviewed the several techniques that have been tried to increase grain size, control grain boundary location, reduce intra-grain defects and control the in-plane orientation of the grains of the polysilicon films. We have discussed the relative merits and drawbacks of the techniques.

The key questions are –1) whether one can get grains, which are single-crystal like with no intra-grain defects by solid phase crystallization, 2) whether the seed and hence the grain location can be accurately controlled, and 3) if the crystal orientation, both vertical and in-plane can be controlled. All these have to be accomplished at low temperature so that it can be used in 3-D IC integration or for displays on glass substrates. We will examine each issue next and suggest some ideas on how these objectives might be achieved.

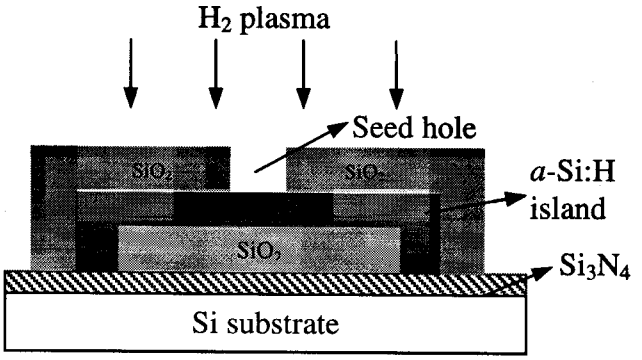
Intra-grain defects and control of grain location

It is well known that defect-free single crystal Si can be realized during vertical SPE. After the surface of a Si wafer is amorphized due to ion implantation, during subsequent anneal the crystal grows vertically from the underlying Si substrate, which acts as seed, to crystallize the damaged portion with no defects. Hence intrinsically

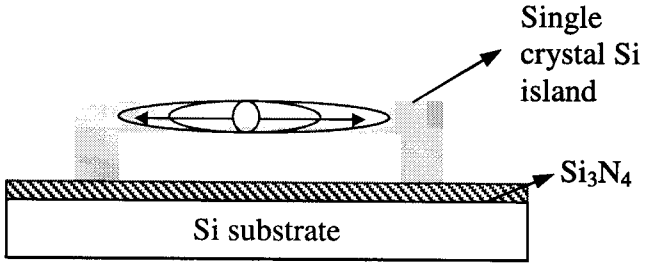
crystalline defects are not created during SPE. However, during LSPE over SiO_2 it was found that defects were created after the crystal growth front extended laterally by ~10 μm from the seed holes (Section 6.3.1). It was speculated that due to volume contraction (from amorphous to crystalline phase) stress is generated at the crystal front, especially at the bottom Si/SiO_2 interface. This stress led to the creation of crystalline defects. Removal of the underlying SiO_2 reduced this stress and defect-free Si could be formed i.e., the LSPE extent could be increased (Section 6.4.1).

During SPC, on the other hand, both nucleation and crystal growth occur. Most of the defects are generated during the initial nucleation stage itself, especially when nucleation occurs at the bottom Si/SiO_2 interface. The number of defects is also increased by contamination like O, C, etc., in the amorphous layers. The stress (due to nucleation at bottom interface) is reduced when nucleation occurs at the top surface, which can easily be achieved by hydrogen plasma seeding. Removing the underlying SiO_2 layer could then further minimize the stress generated during the crystal growth. The grain location can be then controlled by hydrogen plasma seeding at the surface through a mask with small holes (nano-seeds) such that one nucleation seed is created in each hole. During subsequent anneal the crystal growth occurs radially around the seed hole to form single-crystal islands. So we could design a process to incorporate this selective seeding and etch of the underlying SiO_2 to create defect-free Si islands in predetermined locations as illustrated in Fig. 6.2.

The proposed fabrication process is quite similar to that used for surface micromachining in MEMS which is discussed in detail in the next chapter. First create islands of SiO_2 on a Si_3N_4 covered Si wafer. Si_3N_4 is used to alleviate the stiction problem during the etch of the sacrificial underlying SiO_2. Then deposit *a*-Si:H by PECVD or LPCVD (LPCVD might be the preferred technique to minimize



a) Expose to H_2 plasma to create one seed nucleus at *a*-Si surface



b) Remove all SiO_2 and anneal at ~600 °C to realize defect-free single crystal Si island.

Figure 6.2. Schematic fabrication sequence to realize defect-free crystalline Si islands using hydrogen plasma seeding and removal to underlying SiO_2 during crystallization anneal.

contamination in the *a*-Si films during growth) and pattern to form small islands. Then deposit SiO_2 and open small holes in the SiO_2. Expose to H_2 plasma to create seed nucleus (one in each seed hole). Remove the SiO_2, to realize free standing *a*-Si islands with one seed nuclei at the top surface. Anneal the sample at ~600 °C to realize defect-free single crystal Si islands. The variables in the process are: 1) precursor *a*-Si film deposition conditions and thickness, 2) size of seed hole, and 3) size of the *a*-Si islands

Control of crystal orientation

As we discussed earlier (Section 6.5), SPC yields polysilicon grains with predominant <111> vertical orientation. It was also speculated that this was due to the

growth rate difference between the different oriented growth fronts (Fig. 6.1) or due to the fact that <111> oriented surface have minimum surface energy. However, to achieve ideal SOI, both the vertical and the in-plane orientation should be controlled and ideally it should be oriented in <100> direction. We discussed earlier in Section 3.3.8 that <110> and even <100> vertical orientation can be achieved during direct deposition of polysilicon by LPCVD by accurate control of the growth parameters (for e.g., {100} texture could be achieved using silane at 675 °C [75]). We also discussed that the location of nucleation using patterned substrates (Section 6.3.2) can control subsequent growth during poly-Si deposition and this technique was called sentaxy.

We can extend this technique to create crystalline nuclei of Si (<10 nm) at predetermined locations on the substrate (e.g. patterned Si_3N_4 regions on underlying SiO_2, with nucleation occurring preferentially on Si_3N_4 regions) with (100) vertical orientation by LPCVD (HCl might be needed to enhance the selectivity). We can then deposit thin uniform *a*-Si without breaking vacuum so that no native oxide is formed between the nuclei and the *a*-Si layer. Subsequent annealing would realize films with grains having (100) vertical orientation at predetermined locations. This technique is better than continuously growing crystalline silicon as done in sentaxy due to two reasons. First, the films obtained by annealing *a*-Si film deposited on the crystalline nuclei are smoother as direct deposition of poly-Si leads to faceting and hence rougher surfaces. Second, both annealing and deposition of *a*-Si can be done at low temperatures unlike the high temperature (~1000 °C) used during sentaxy. The variables in this process are: 1) exact growth conditions to realize grains with <100> vertical orientation, 2) substrate preparation and cleaning and the growth conditions required to enhance the selectivity so that nucleation occurs preferentially on the Si_3N_4, 3) duration

of growth so that only one crystalline nucleus is formed, and 4) growth conditions to deposit *a*-Si by LPCVD and the thickness of the film.

These are just a few ideas that could possibly be used to achieve the goal of SOI films. There are several groups all around the world, working in this field optimizing the specific process they have developed and extending them so that better performance can be achieved. Depending on the application and specific requirements of the end user, of one of the several techniques might be applicable. In addition to the methods described here laser crystallization of *a*-Si to achieve similar objectives has been gaining attention over the past few years.

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Chapter 7

MICRO-ELECTRO-MECHANICAL CHARGE-SENSING DEVICES FOR PLASMA-PROCESS-INDUCED CHARGING DAMAGE MEASUREMENT

7.1 INTRODUCTION

Plasmas are being widely used in the semiconductor industry for delineation of fine line pattern and deposition of either semiconducting or insulating layers at low temperature. In recent years, it has been reported that plasma nonuniformity across the wafer plays an important role in charging damage [1]. The plasma nonuniformity due to nonuniformities in radio frequency (RF) current flow [2], electron current flow [3], and ion current flow [4] can cause significant charging of surfaces. Charging also occurs when fine features are etched with high aspect ratio photoresist masks, even if the plasma is uniform, due to electron shading effect [5]. This plasma related charging can severely degrade or destroy devices, especially Metal Oxide Semiconductor (MOS) gate dielectrics [6]. This particular problem is becoming more important as gate oxides become thinner and hence more vulnerable to this surface charging [7].

The charging damage is most severe during the plasma etching steps, viz., during the gate definition step [8], when the gate stack is etched and the etch is terminated at the gate oxide of the MOS transistor, and during any subsequent metal patterning step with the metal being connected to the gate of the transistor and the metal exposed to the plasma during the etching step (antenna effect) [9]. When placed in the plasma, the wafer surface reaches a potential at which there is a balance between the ion current and the time-averaged electron current. From the point of view of gate oxide stressing, the degradation occurs when the potential difference across the oxide is high enough to cause Fowler-Nordheim (FN) tunnel injection between the gate and the silicon substrate. During plasma exposure, the gate potential adjusts itself so that the plasma-charging current, equal to the difference between the ion and electron current, is balanced by the FN tunneling current. The flow of tunneling current generates trap and interface states in the gate oxide, causing deterioration of the oxide quality and integrity. At very high level of stress or prolonged exposure, it may also ultimately lead to the breakdown of the oxide [10].

As a typical modern integrated circuit (IC) fabrication involves many plasma processes, quantifying the damage caused to the device at each step and singling out the process leading to charging damage are difficult. Most of the conventional techniques to determine damage involve either indirect techniques like measurement of the degradation of the various characteristics of the transistors [11] (hot carrier reliability, threshold voltage, subthreshold swing, etc), or the capacitors from different splits with varying process conditions, and then estimating the damage from a single process step. The plasma damage can also be determined by using invasive techniques like Langmuir probes [12] (metal electrode inserted into the plasma) or MOS capacitors with wires running out of the plasma chamber [13]. These can perturb the plasma and therefore the

conditions under which the charging is determined need not be the same as those during the actual processing. EEPROM transistors with floating gates have also been used to determine the charging damage. The damage is then inferred from the threshold voltage shift of the transistor due to the charge trapped in the floating gate (CHARM sensor) [14, 15].

In this chapter we will discuss a device which can *non-invasively* measure this charging *in-situ*, in real time, in the plasma reactor, as opposed to the conventional method of inferring the charge from later measurement of device degradation or using wires and probes or other elements which may perturb the plasma. Our method can also be used to quickly map charging across the electrode. The charging is measured *in-situ* by measuring the deflection of micro-cantilevers.

7.2 PLASMA-INDUCED CHARGING: AN OVERVIEW

Damage to gate oxide and SiO_2/Si interfaces due to plasma processing is a major concern for the advanced submicron MOS technologies. Interlayer dielectric deposition and etching, polysilicon gate definition, and contact and via etch require an increased number of plasma-based process steps which can cause damage to transistor gate oxides and their interfaces with Si. This damage is believed to arise through several mechanisms:

(1) current flow stress due to charging,

(2) plasma-induced photon and particle bombardment,

(3) unwanted chemical reactions, and

(4) impurity deposition and subsequent permeation.

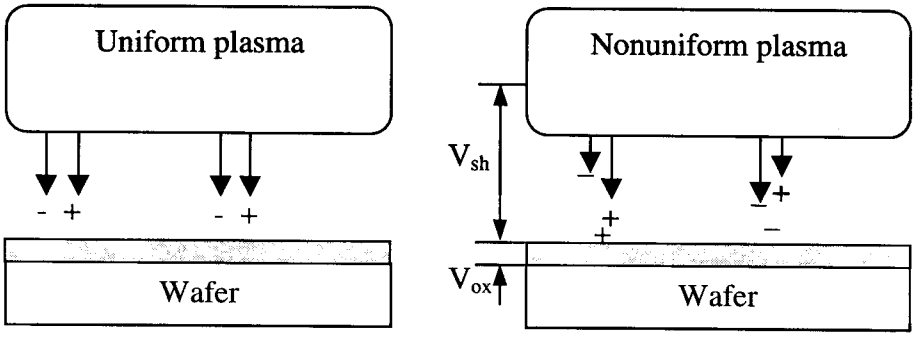
Of all the plasma related damage mechanisms that have been studied so far, oxide-charging damage has been recognized to be the most significant [11]. The oxide charging can occur due to nonuniform plasmas or due to electron shading, which occurs even in

uniform plasmas when topology is present on the wafer. In the following sections, we will discuss these plasma-charging mechanisms, and the techniques used to study and minimize their effects.

7.2.1 Causes of plasma-induced charging

Plasma nonuniformity

A wafer in contact with plasma is subject to electron and ion bombardment. In uniform plasma, these fluxes or currents are locally balanced over each RF cycle everywhere over the wafer surface as shown in Fig. 7.1(a). Charging is not a problem and the surface potential stays close to that of the substrate. However, most processing plasmas are not totally uniform across the wafer surface in terms of plasma density (n_e and n_i) and plasma potential (V_p). This nonuniformity leads to local imbalances in the electron and ion currents, at least initially, as shown in Fig. 7.1(b). If the surface is a conductor, surface currents flow to balance these currents. If the surface is an oxide or a discontinuous conductor (gates, or during overetch of metals/poly-Si) on an oxide, the surface charges in such a direction so as to bring the local electron current into balance with the local ion current. This results in a voltage V_{ox} (x, y) across the oxide [6]. To understand this further, we will look at the plasma currents and voltages in more detail. A plasma is made up of two regions. The central glow region, often referred to simply as the plasma, is quasi-neutral and has resistivities in the range of 10^2 to 10^7 ohm-cm depending on the gas and discharge conditions. Between the plasma and all the surfaces, there is a boundary region called the sheath, which is an electron depletion region that forms to retard the more mobile electrons from leaving the plasma faster than the ions can. Due to the lack of electrons in the sheath, its impedance is high in comparison to the plasma, and most of the voltage drop in the discharge occurs across the sheath. For this reason, the plasma region is characterized by a single voltage



(a) Minor charging (b) Charging

Figure 7.1. A schematic model showing the wafer charging for oxide exposed to (a) an uniform plasma, and (b) oxide exposed to a nonuniform plasma at the initial state, where V_{sh} is the sheath voltage, and V_{ox} is the oxide voltage [6].

V_p, which is called the plasma potential. In a nonuniform plasma, V_p is a function of position. For an RF driven discharge, V_p has the form $\bar{V}_p$ +Asinωt. The sheath is given by (Fig. 7.1(b))

$$V_{sh} = V_p - V_{ox} - V_{wafer} \qquad (7.1)$$

The positive ion current J_i is equal to the ion impingement flux at the plasma/sheath interface and is given by [17]

$$J_i = 0.6qn_i u_B \qquad (7.2)$$

where u_B is the Bohm velocity, which is a function of the electron temperature in the plasma. The electron current is reduced from its sheath impingement flux by the sheath barrier and is given by [17]

$$J_e = 0.25qn_e u_e e^{-\frac{qV_{sh}}{kT_e}} \qquad (7.3)$$

where $u_e = \sqrt{8kT_e/\pi m_e}$ is the electron mean thermal velocity and electrons are assumed to have a Maxwell-Boltzmann distribution in the plasma, characterized with an electron temperature T_e. The exponential dependence of J_e on V_{sh} means that J_e only flows during the part of the RF cycle that V_{sh} is near its minimum. If we assume that the V_p

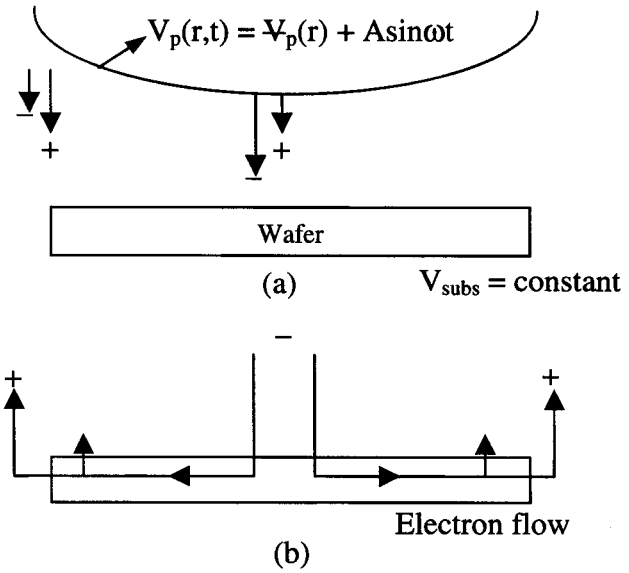


Figure 7.2. A schematic diagram showing (a) how the local ion/electron current imbalance occurs from a nonuniform plasma. J_e is larger at the wafer center than at the edge because of the smaller electron barrier (V_{sh}) at the center, and showing (b) electron flow across the entire wafer at steady state [16].

amplitude A is constant across the wafer, J_e dominates where $\bar{V}_p$ is near its spatial minimum and J_i dominates where $\bar{V}_p$ is near maximum as shown in Fig. 7.2(a). This tends to be true independent of the spatial variation of plasma densities, since density only has a linear effect on J_e and J_i. Since V_{sh} depends on V_{ox} (equation 7.1), there is a feedback in the surface charging which adjusts the local J_e toward the local J_i.

For thin oxides the surface stops charging at the point when the local net particle current ($J_i - J_e$) equals the local Fowler-Nordheim (FN) tunneling current through the oxide. Here the balance is achieved by across-the-substrate currents (Fig. 7.2(b)). Damage occurs when the net fluence of the FN current approaches the charge-to-breakdown Q_{BD} for the oxide at the processing temperature. The damage is enhanced if there is a gate extension over field oxide where all the collected current is fed to the thin oxide. This collection is the so-called "antenna" effect.

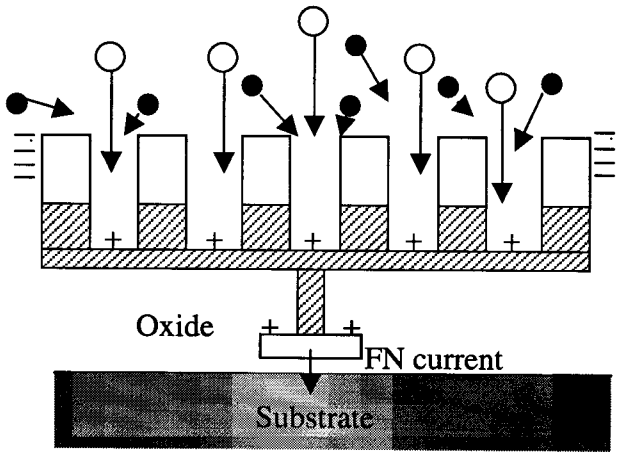


Figure 7.3. Schematic cross-section at a moment near endpoint of dense-line pattern etching, showing the electron shading effect, with anisotropic ions reaching the spaces while the isotropic electrons are shielded by the mask. The open circles represent ions, and the closed symbols electrons [5].

Electron shading

Some workers have recently reported a new kind of charging phenomenon termed as "electron shading", which occurs even in uniform plasmas when topography exists on the wafer during plasma exposure [5]. Electron shading is caused by the difference in directionality of electrons and ions crossing the plasma sheath to the wafer surface. In high-aspect ratio spaces, isotropic electrons are shaded; that is, they are hindered from reaching the bottom of the space, whereas anisotropic (and positively charged) ions are not (Fig. 7.3). Insulators such as photoresist or oxide are commonly used as masks when etching conductive films, so that the underlying conductor can acquire a positive charge by the electron shading mechanism. This problem is generic to high-density plasma etch tools [5] and is more severe in modern IC processing with high density of features to be etched.

7.2.2 Techniques to evaluate charging in plasmas

A variety of techniques exist to evaluate the gate oxide damage during plasma processing and they fall in two broad families of measurement techniques: those that

Technique	Measure charging source	Measure charging effect
Examples	EEPROM/CHARM-2, MNOS, SPORT, MEMS charge sensor, surface charge analysis, contact potential difference	Device parameter degradation of antenna capacitors/transistors or actual devices
Strengths	Fast Independent of gate oxide quality Isolates charging source	Real topography and structures Processes are fully integrated
Weaknesses	Wafer topography and structures may not match real devices Looks at isolated, not integrated processes	Slow Dependent on gate oxide quality Difficult to precisely isolate charging source
Uses	Plasma tool development and characterization Process optimization	Process integration Overview of charging sources and trends

Table 7.1. Comparison of plasma-induced damage measurement techniques.

characterize the charging source independent of the gate oxide and those that characterize the effect of the damage by examining gate oxide degradation (Table 7.1).

Measurement of charging source

To study the damaging potential of the plasma itself, measurement devices include EEPROM transistors, metal-nitride-oxide-semiconductor capacitors and transistors, and direct measurement techniques. Of these, the most commonly used was EEPROM transistors commercialized as CHARM-2 (CHARge Monitor) wafers by Wafer Charging Monitors [14, 15]. This technique relies on the shift in the threshold voltage that occurs when a high potential is applied to the control gate of the floating gate EEPROM. MNOS transistors/capacitors are also used commonly, with an approach similar to that of EEPROM [9]. An important capability of EEPROM transistors is the measurement of the plasma characteristic, which is the current density-voltage curve (J-V) of the plasma. This is accomplished by adding current-sensing resistors between the

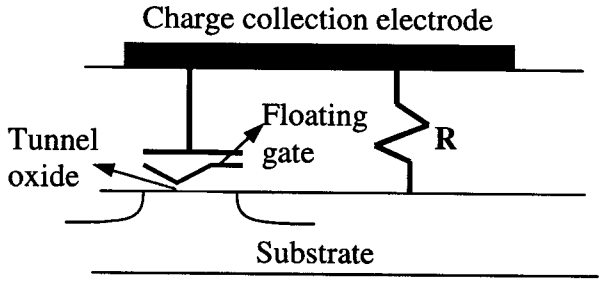


Figure 7.4. Schematic diagram of the cross-section of the CHARM-2 charge sensor with a resistor connected in parallel to the EEPROM transistor between the charge collection electrode and the substrate [15].

charge collection electrode on the surface of the wafer and the substrate (Fig. 7.4). In this configuration, the EEPROM transistor is used to measure the voltage across the current-sensing resistor, from which the current density may be determined. By varying the value of the resistors, the J-V characteristics of the plasma can be easily determined [15] (Fig. 7.5). Knowing this characteristic and the current-voltage characteristic of the gate oxide, one can predict how the plasma will interact with the oxide.

Recently, techniques such as surface charge analysis and contact potential difference [18] as well as direct measurement of charging (for instance, Stanford Plasma On-wafer Real-Time, or SPORT [19], measurements) have been more widely used to study the charging potential of plasmas. The SPORT technique involves the measurement of current-voltage curve of a MOS capacitor with ~1-μm thick dielectric exposed to the plasma [13, 19]. The SPORT technique requires some hardware modification as the measurement is made via wires attached to the gate and the substrate of the capacitor, but has the advantage of giving in-situ real-time results for rapid plasma optimization [19]. FLASH memory cells have also been used as a charging sensor [20].

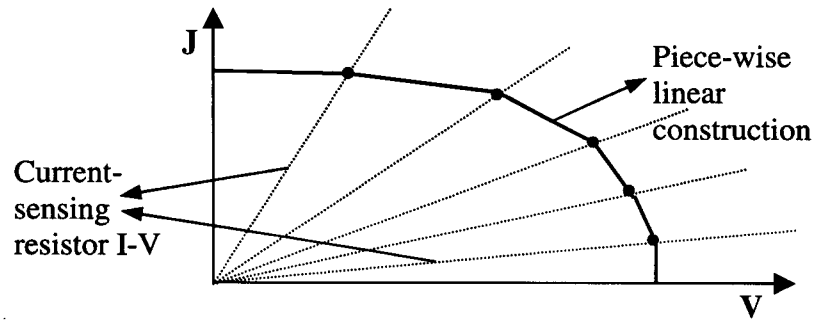


Figure 7.5. CHARM-2 charge sensors with different value of charge-sensing resistors allowing the reconstruction of the J-V characteristics of the charging source [15].

Measurement of charging effect

To study the effect that plasma damage has on the gate oxide, electrical parameters are measured appropriate for capacitors or transistors, which are typically connected to large conductive antennas over thick field-oxide. A wide variety of device parameters have been used to characterize the damage, but the most common parameters include breakdown voltage, flat-band voltage and interface-state density for capacitors, and gate leakage, threshold voltage shift, charge-to-breakdown and hot carrier degradation for transistors. Measurements are generally considered to more accurately reflect actual damage of real devices when F-N stress is used to draw out the latent damage, which has been hidden by hydrogen passivation during the forming gas anneal, but which will reappear as the device is operated [21].

7.2.3 Techniques to minimize plasma-induced charging damage

There are four general strategies one can follow to reduce gate oxide damage: improving the damage source, reducing the device exposure to damage, improving device resistance to damage and removing damage after it has occurred (for instance, by increasing the annealing temperature [22] or by reoxidizing the gate oxide that has been physically damaged at the gate edges).

Reduce source of damage

An obvious way to reduce the source of damage is to select the least damaging equipment or modify an existing piece of equipment. Besides changing the hardware, the process can be changed as well: processes should be optimized for damage just as they are for providing the best profile, the best uniformity or the best control of critical dimensions. Trade-offs are required to achieve the overall optimized performance. Examples of hardware and process improvements include: turning off plasma source power prior to bias power when etching is complete [23] to reduce transient currents during power turn-off, reducing the electron temperature (reduces electron shading effect) by decreasing the source power and increasing the bias power [24] or by plasma pulsing [25], or increasing the gap between the wafer and the upper electrode [26]. Failures can increase by an order of magnitude when the processing temperature is increased, for it is well known that the dose required to breakdown an oxide (charge-to-breakdown or Q_{BD}) decreases with temperature [27, 28]. So even small amounts of charging may be sufficient to destroy gate oxide when a high-temperature plasma etch or deposition step is used [29]. Processes that operate at reduced temperature, therefore, can be expected to be less sensitive to charging.

Reduce exposure of device to damage

The exposure of a device to damage can be reduced by imposing "antenna" design rules, such as limiting the area of a polysilicon line to be no more than 100 times as large as the area of the gate oxide it covers. Reducing etch mask thickness was found to reduce damage, probably by limiting the electron-shading mechanism due to the reduced aspect ratios [30]. Damage-reducing features, such as using a protective dielectric [31], can be incorporated into the process architecture. Reverse-bias-protection diodes can be added into the circuit design to shunt current away from the sensitive devices [32]. As

the oxide thins, however, the challenge increases to keep the source/drain junction breakdown voltage of the diode below the gate oxide breakdown voltage of the device being protected, even with assistance of light from the plasma, unless the diode area increases [32, 33].

Increase resistance of device to damage

Gate oxide damage can also be reduced by improving the resistance of the gate oxide to damage. This can be accomplished by either reducing defects in the gate oxide, for instance, those introduced by the use of boron implantation to form p^+ gates [34], or by improving the gate oxide integrity. One technique for improving integrity is to grow the oxide in an N_2O ambient rather than a pure O_2 ambient [35].

Much work remains to be done, however, to learn how to create the strongest gate oxide, the least susceptible circuit designs and the gentlest plasma tools and processes to control gate oxide damage from plasma processing.

7.3 MEMS CHARGE-SENSING DEVICE

In this section, we will discuss the principle, the fabrication, and the operation of a micro-electro-mechanical charge-sensing device to evaluate the charging in plasmas non-invasively and directly without the use of wires or probes [36]. This technique falls under the category of "measuring the charging source" in Table 7.1.

7.3.1 Concept

A microscopic cantilever made from a conducting material, suspended above and electrically isolated from a conducting surface, can act as a charge-sensing structure. If an interaction with plasma or fluid were to add electrons or ions to the cantilever surface, the cantilever would become charged. The substrate would mirror that charge, resulting in an electric field between the cantilever and the surface below

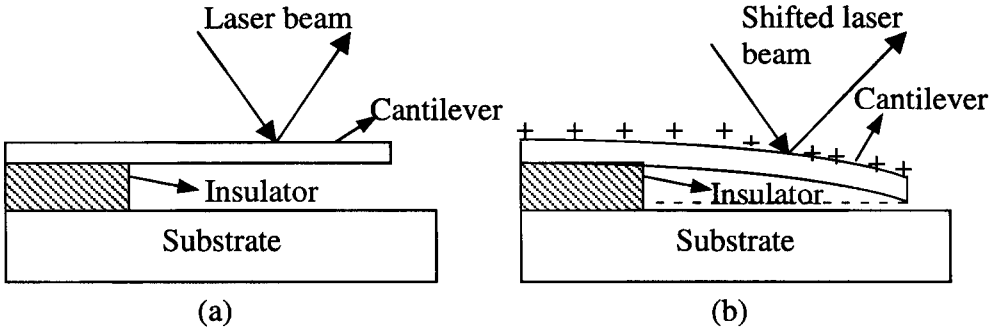


Figure 7.6. Microscopic charge-sensing structure for (a) uncharged and (b) charged surfaces.

and hence causing deflection of the beam as shown in Fig. 7.6. The beam would deflect towards the substrate for either positive or negative charge. The deflection may be measured by the shift in the reflected spot of a laser probe caused by the change in the angle of reflection of the laser beam, and the charge on the cantilever can be calculated from the deflection.

Experimentally, the use of cantilevers might be difficult since the angle of deflection varies along the length of the cantilever, and focusing a laser beam onto a small portion of the cantilever inside an etching reactor might be difficult. Therefore, we modified the cantilever concept to fabricate paddles [37] (Fig. 7.7(a)) or torsional mirrors[38] (Fig. 7.7(b)), where a large area is connected to the support by thin arms. In these structures, the sensitivity was enhanced compared to cantilevers, the angle of deflection was nearly constant over most of the reflecting area, and the laser beam covered several adjacent identical paddles. Various sizes of these structures were made so that each paddle detects a particular range of voltage.

7.3.2 Modeling

The deflection behavior of these cantilevers/paddles as a function of the applied bias was modeled by first assuming the cantilever/substrate to be a parallel plate

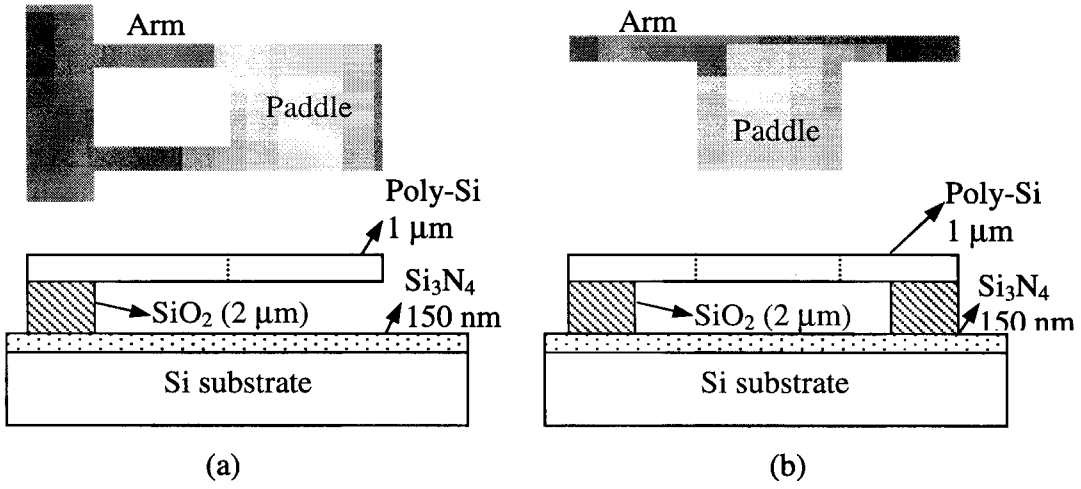
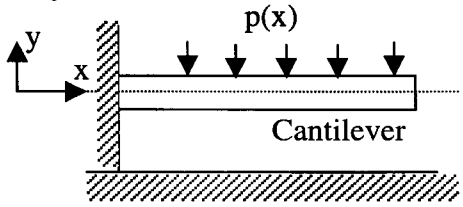


Figure 7.7. Schematic diagram of the top and side views of (a) paddle structure, and (b) torsional mirror, with the thickness of the different layers indicated.

capacitor and then calculating the force on the cantilever for an applied voltage. The Finite Difference Method was used to solve the fourth order differential Euler's equation to estimate the position of cantilever and therefore the deflection angle for every applied voltage. This modeling was done prior to the actual design of the masks for the fabrication. We needed to optimize the size of the devices so that each device responds to a different range of applied voltage.

From basic mechanics (Euler's equation of beam deflection), neglecting shear deformation and assuming perfect elasticity and at steady state, we have [39, 40]

$$EI\frac{d^4y}{dx^4} = p(x,y) \qquad (7.4)$$



where y is the deflection (height) cantilever, E is the Young's modulus of elasticity of the beam, p is the electrostatic force at each point due to the applied bias, and I is the moment of inertia about the neutral axis of deflection. The boundary condition is that the deflection at the fixed end is zero. I for a cantilever is given by $bt^3/12$ where b is the

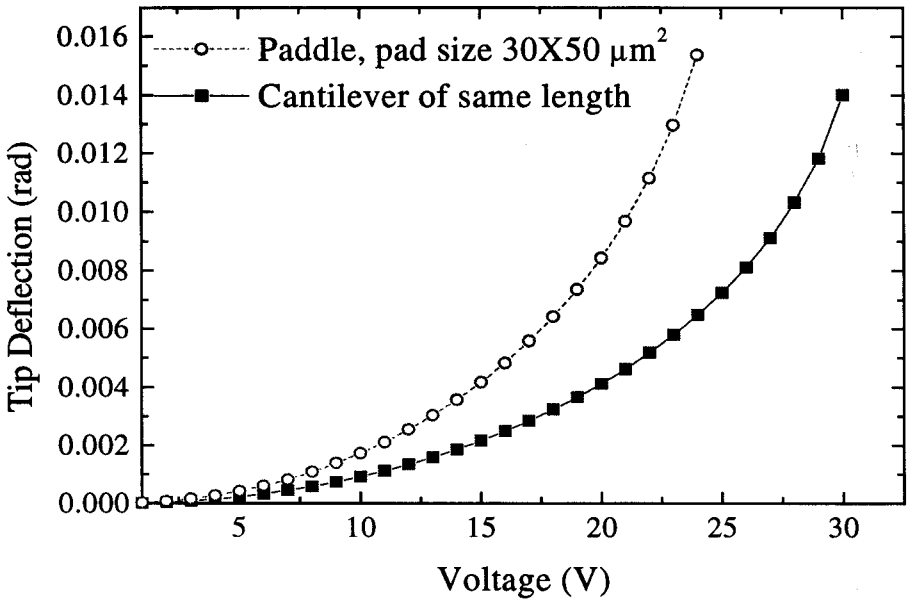


Figure 7.8. Tip deflection vs. voltage for the paddle structure and a simple cantilever of the same length (simulated).

beam width and t is the thickness of the beam. The force p acting on the beam (similar to that experienced by a parallel-plate capacitor) can then be approximated as

$$p(x,y) = -\frac{\varepsilon_o b V^2}{2y^2} \qquad (7.5)$$

where ε_o is the permittivity of free space, b is the beam width, V is the external applied bias and y is the separation between the cantilever beam and the substrate plane. The parallel plate approximation is used in this case and fringing fields, if any, are neglected. Equation (7.4) can also be written as [40]

$$EI\frac{d^2y}{dx^2} = M(x,y) \qquad (7.6)$$

where M is the total bending moment at location x due to the electrostatic force. Using equation (7.5), equation (7.4) can then be rewritten as

$$\frac{d^4y}{dx^4} = -\frac{k}{y^2} \qquad (7.7)$$

with $k = \varepsilon_o bV^2/2EI$. The fourth order differential equation (one-dimensional) can be then numerically solved by dividing the beam in one dimension into sections and using the midpoint (central) difference between the sections to estimate the differential as

$$\frac{d^4y}{dx^4} = -\frac{y_{i+2} - 4y_{i+1} + 6y_i - 4y_{i-1} + y_{i-2}}{h^4} = -\frac{k}{y_i^2} \qquad (7.8)$$

where $h = (x_{i+1} - x_{i-1})/2$. Equation (7.8) can then be recast as a matrix equation. The y_i's can then be determined by iteratively solving the equation (7.8) for a given external bias from the initial condition when the cantilever is unbent and all the y_i's are equal.

Simple cantilevers (Fig. 7.6(a)) and structures with larger reflecting areas like paddles (Fig. 7.7(a)) and torsional mirrors (Fig. 7.7(b)) were modeled by the technique described above. As can be seen from Fig. 7.8, the paddle structure has a smaller pull-in voltage than a simple cantilever of the same length, demonstrating the increased sensitivity that can be achieved with the paddle modification. The dimensions of the devices were varied and the tip deflection angle was plotted for various applied voltages (Figs. 7.9(a) and 7.10(a)) so that a wide range of charging voltages can be measured. The position of the beam (or paddle or mirror) along the neutral bending axis was also calculated to determine which structure has least distortion and the most area/length with the deflection angle being constant. Fig. 7.9(b) shows the vertical position of the paddle along the length of the device for various voltages, with the cantilever deflection at 26 V also shown for comparison. It clearly shows that the paddles region is nearly flat with a constant deflection angle and that most of the bending occurs in the thin support arms, unlike the cantilever, which bends all along the length. The torsional mirror, on the other hand, shows significant bending of the thin support arms (in

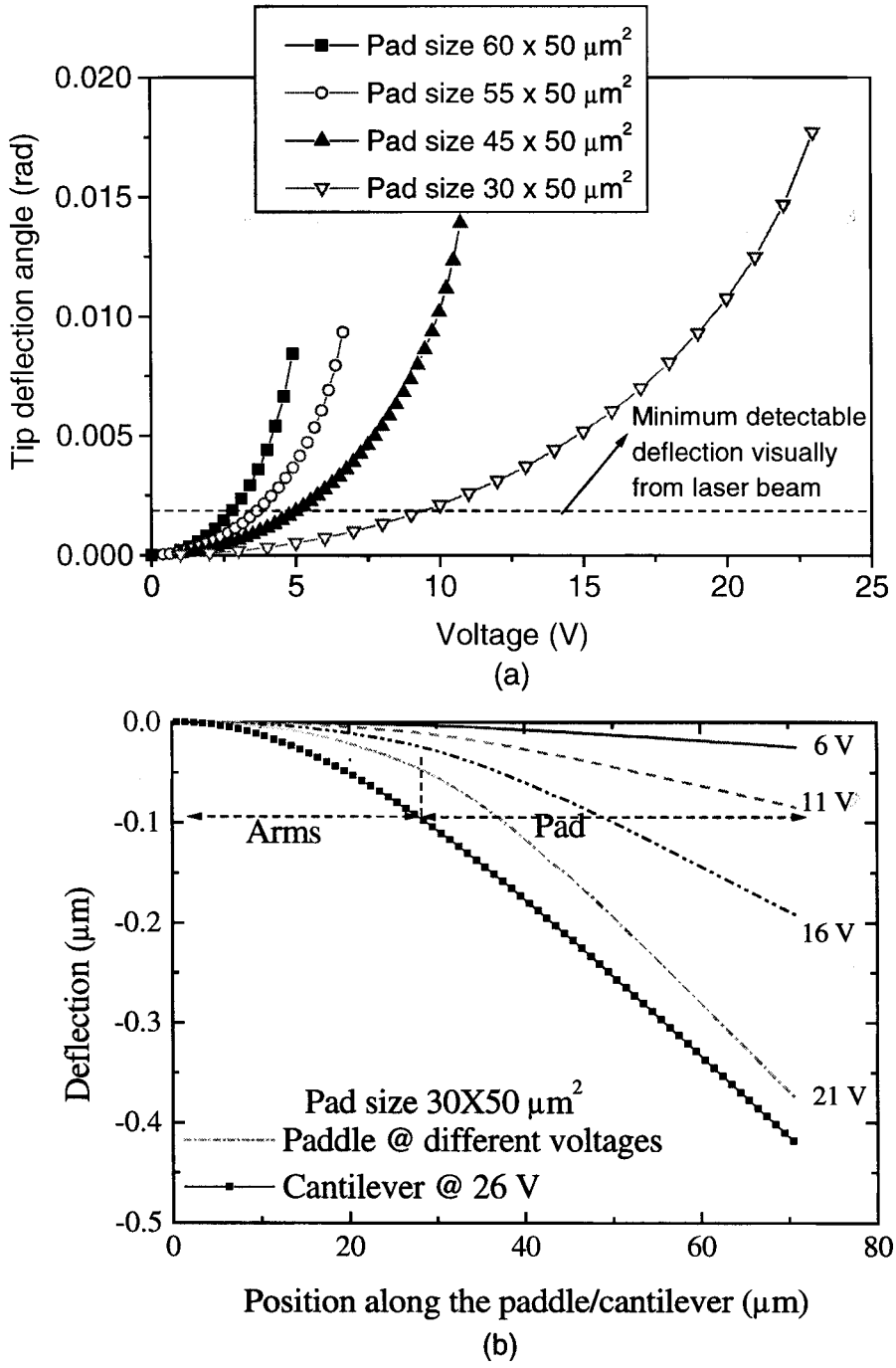
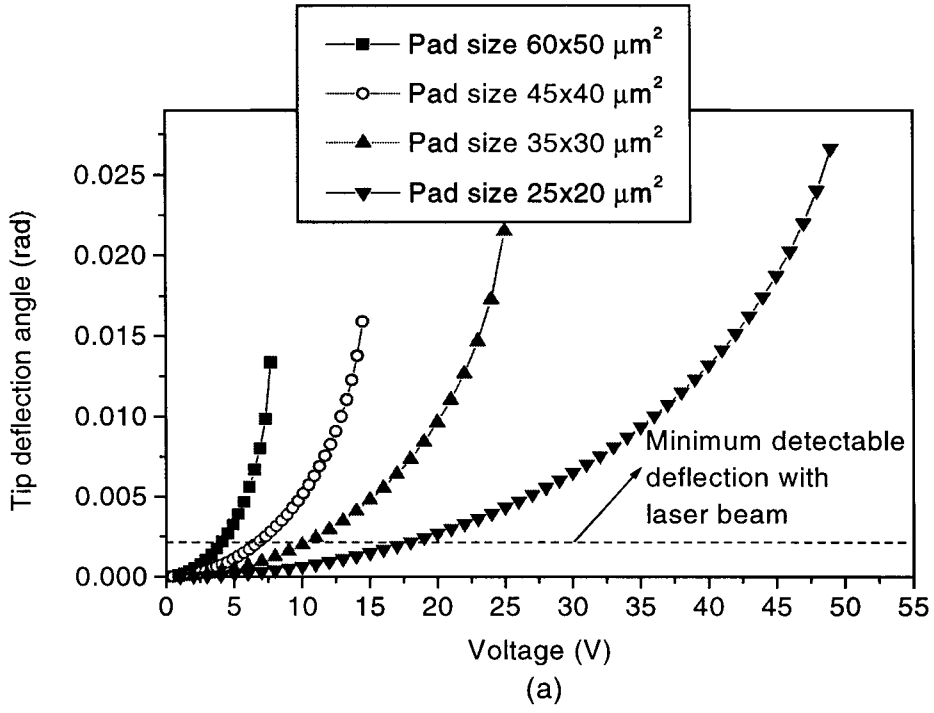


Figure 7.9. Simulation results of the paddle structure, (a) tip deflection angle as a function of the voltage bias between the polysilicon and the substrate for various sizes of paddles, and (b) side-view of the deflection of the paddle structure at various biases with the deflection of the cantilever shown for comparison.



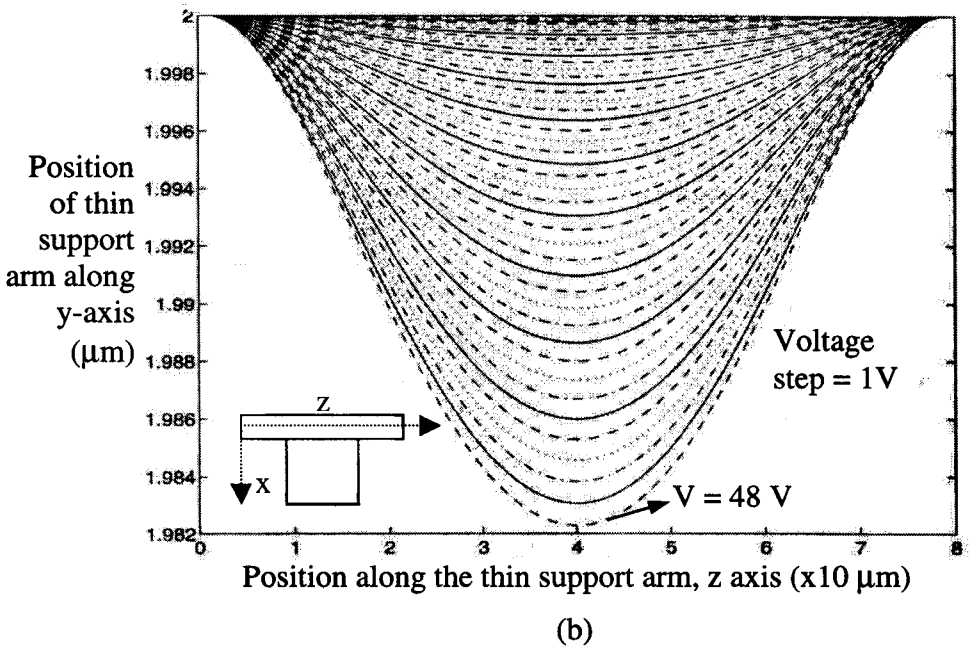


Figure 7.10. Simulation results of the torsional mirror structure, (a) tip deflection angle as a function of the voltage bias between the polysilicon and the substrate, and (b) side-view of the deflection of the support arm for various biases.

addition to twisting which is desired) and therefore leading to distortion (Fig. 7.10(b)). The flatness of the paddle-like structure is crucial, as the deflection angle is determined from the shift in the laser beam reflected spot. In practical applications, it might be difficult to focus the laser beam spot right at the tip of the cantilever, and if the deflection angle varies along the cantilever beam, the read-out from the laser will be erroneous. From our modeling data, the paddle structure was determined to have the best characteristics in terms of least distortion of the paddle itself (constant deflection angle) and large range of sensitivity to the applied voltage bias. The reflecting pad areas of the paddles finally chosen, range from 60 μm x 50 μm to 30 μm x 50 μm with arm lengths from 40 μm to 30 μm, and nearly all structures had an arm width of 10 μm with a few devices having an arm width of 5 μm. The dimensions of all the paddle structures are designed for a sacrificial layer etch duration of about 4 h.

7.3.3 Fabrication details

The paddle structures and the cantilevers are fabricated by standard surface-micromachining technique. Fig. 7.11 shows the fabrication sequence. N^+-type silicon wafers (0.5-2.0 Ω-cm) are used as substrate. First, a layer of silicon nitride of thickness 150 nm is deposited by chemical vapor deposition (CVD). This serves to alleviate "stiction" problems during processing. Stiction occurs when the cantilever deflects all the way and sticks to the substrate. The second step involves creating the sacrificial layer, which will be isotropically etched to realize freestanding structures. In this case, a 2-μm thick silicon dioxide (SiO_2) layer is deposited by atmospheric pressure CVD. A 1-μm thick polycrystalline silicon layer is then deposited by low-pressure CVD and is doped heavily with phosphorus (~10^{20} cm^{-3}) to have high conductivity, and annealed to reduce the internal stress [38, 41] in the polysilicon cantilevers (Fig. 7.11(a)).

The polysilicon is first dry etched in SF_6 plasma (RF power of 30 W, pressure 150 mtorr & flow rate 15 sccm) till the underlying SiO_2 is reached (Fig. 7.11(b)). This plasma-etch chemistry has a very high selectivity (~30) of Si etch versus SiO_2 etch, hence overetch can be tolerated. Next photoresist (AZ1518) is spin-coated on the support structure to prevent the silicon dioxide underneath the support from being etched during the release step (Fig. 7.11(c)). The etch-release step involves sacrificial layer etching of SiO_2 in buffered HF (BHF) acid for ~4 h. Even though the BHF etches SiO_2 nearly equally in the vertical and horizontal directions (etch rate ratio in vertical and horizontal direction is 1:0.8), the BHF solution is continuously stirred mechanically to aid the etching of the SiO_2 underneath the polysilicon cantilevers (Fig. 7.11(d)).

Photoresist adhesion improvement

If the photoresist (AZ1518) did not adhere to the support well during the spinning/curing step, during the HF etch the photoresist lifts up at the corners leading etching of SiO_2 under the support column. This results in the whole polysilicon structure being etched off. To ensure better adhesion of the photoresist to the applied surface extensive surface preparation steps and a few changes in the standard photolithography process were required. First the surface is dried (minimize –OH at the surface which hinders adhesion of photoresist) by heating the sample at 130 °C on a hot plate for ~10 min. Then a few drops of hexamethyldisilicate (HMDS), which is an adhesion promoter, are applied on the sample with the sample on the hot plate. After some of the HMDS has vaporized, the rest of the HMDS is spin-coated on the sample. Immediately afterwards, the photoresist is spin-coated and pre-baked at 110 °C for ~2 min. The sample is then exposed to UV through the mask to realize the features. Before the developing step, the sample is heated at 110 °C for ~1 min. The features are then developed, as done normally, in AZ400K developer diluted with deionized (DI) water

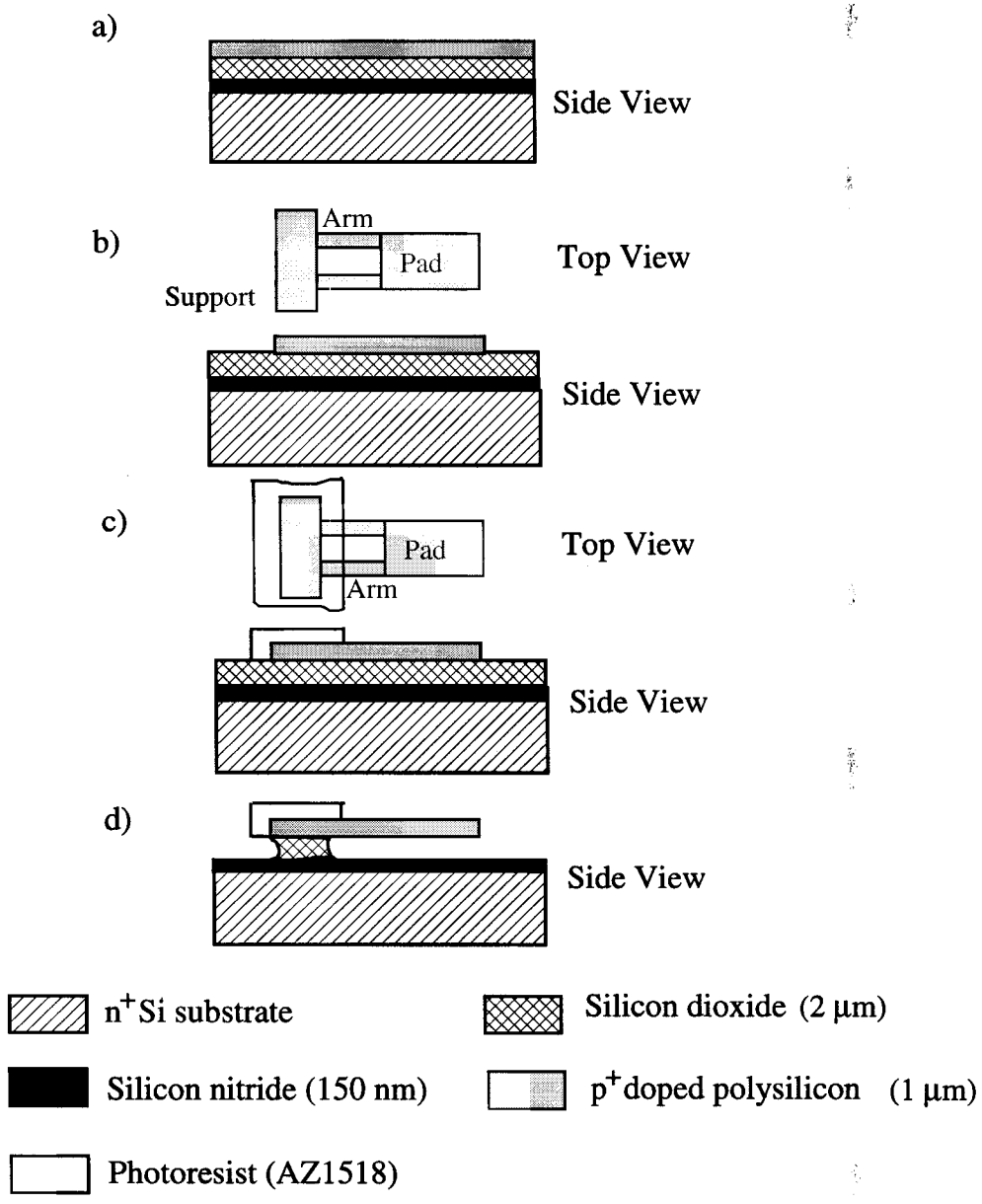


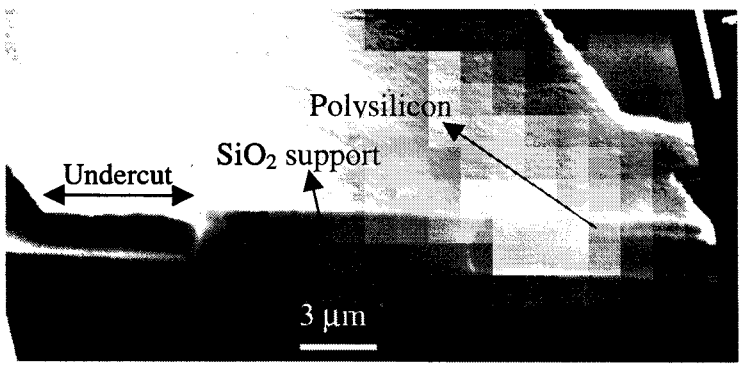
Figure 7.11. Schematic illustration of the fabrication process sequence of the paddle structure, (a) cross-section of wafer used, (b) dry etch the polysilicon, (c) spin-coat photoresist to protect the SiO_2 underneath the support during the release step, (d) after the SiO_2 underneath the paddle structure has been etched off, with the photoresist on the support to be removed by rinsing in acetone.

(1:3.5) for ~30 s. The sample is then post-baked at 110 °C for ~10 min to harden the photoresist and make it impervious to the etchant. The sample is then placed in 6:1 BHF solution to etch the underlying SiO_2 and release the cantilevers. In spite of all these steps, significant etching of the SiO_2 underneath the support did occur as can be seen in the scanning electron micrograph (SEM) shown in Fig. 7.12(a).

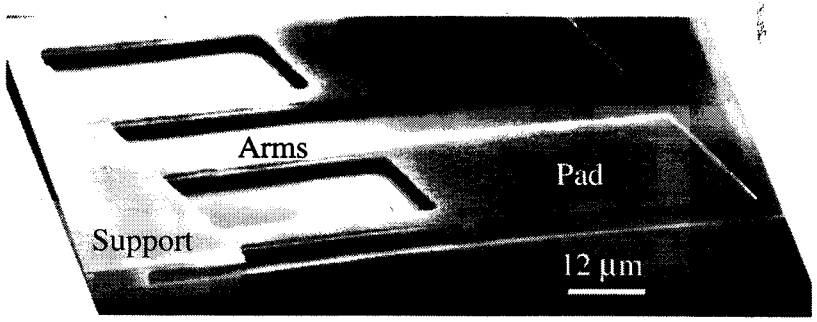
Drying

After the etch is completed (~4 h), the sample is then carefully rinsed in DI water by placing the sample without the water being allowed to dry in a beaker with clean DI water. After several such rinses, the sample is placed in a beaker with acetone to remove the photoresist. Drying the wafers under atmospheric conditions leads to stiction [42, 43]. Due to surface tension force, the drying liquid pulls the cantilevers all the way towards the substrate. The HF etching step leaves a fluoride residue at the underside of the cantilever and the substrate surface, and if the cantilevers bend all the way to the substrate during the drying step, they remain stuck due to the fluoride residue [43]. Hence, various drying methods were attempted to alleviate this stiction problem, like vacuum drying [38] and drying the wafer on a hot plate [44].

The vacuum drying method involves the following steps. After the HF has been rinsed off with DI water, the sample in placed in a beaker with 20:1 of isopropyl alcohol: DI water. The sample is then placed face up in a simple vacuum system (with just a roughing pump) without the alcohol mixture being allowed to dry. A few more drops of the mixture are added on top of the surface until it runs off the surface. The chamber is pumped right away. The pressure goes down to ~0.6 torr, while the water and then ice is evaporating. The ice actually sublimates. As the alcohol evaporates quickly in vacuum, it cools the sample and the remaining water freezes. The ice then sublimates. After ~30 min, the ice is all gone and then the pressure goes down to the



(a)



(b)

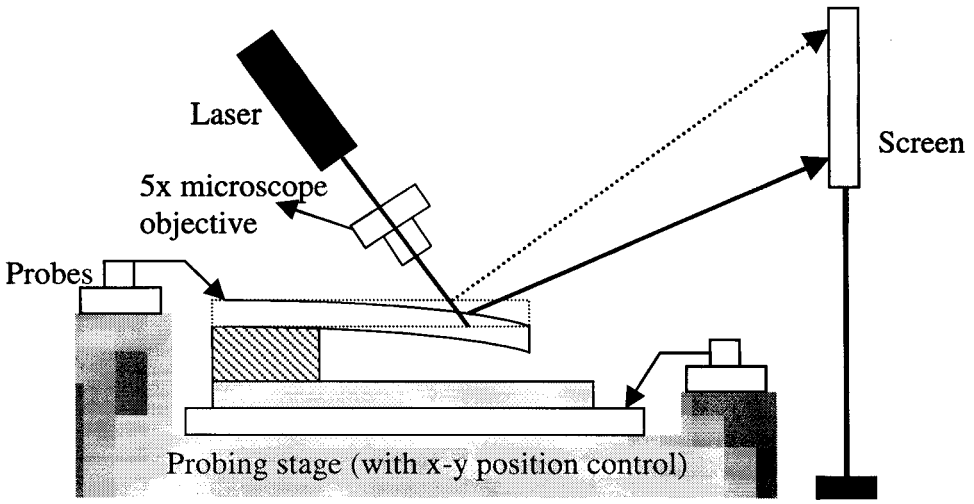
Figure 7.12. Scanning electron micrographs of the cross-section of the MEMS charge sensor after completion of fabrication, (a) undercut of the SiO_2 underlying the support, and (b) view of the complete paddle structure after the release step.

base pressure of the system (~70 mtorr). The sample can then be taken out. The yield with this method was less than 50 % and the procedure was time consuming. However, the second method gave better results. It involved soaking the wafer in pure isopropyl alcohol for 10 min after the DI water-rinsing step until the alcohol displaces all the water underneath the paddles. The alcohol on the backside is removed by placing the sample on absorbing paper. Then the sample is placed on a hot plate at 200 °C with a glass slide in between the hot plate and the sample. The alcohol quickly evaporates within ~15 s. This process has much larger yields (up to ~90 %). Care has to be taken during this process to ensure that the alcohol does not dry before the evaporation step. Fig. 7.12(b) shows the SEM of the completed device after the drying step.

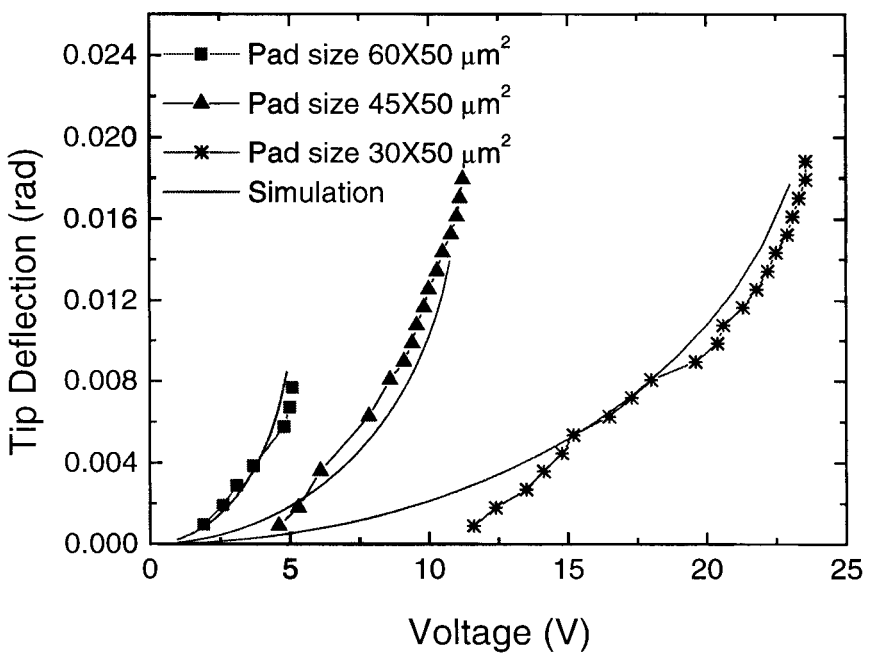
7.3.4 Results and discussion

External calibration

Prior to exposure to plasma, the devices are externally calibrated by observing the deflection in response to an applied electrical voltage, using a needle probe to apply voltage to the polysilicon on top of the support. The laser beam spot was reduced to ~5 μm diameter by using a microscope objective (5x), so the laser beam can be focused using a x-y-z micrometer stage, on to a particular cantilever (or a particular region of the paddle). A special probing stage was constructed so that data for several devices could be easily taken in this fashion (Fig. 7.13(a)). Fig. 7.13(b) shows the tip deflection angle of the paddle as a function of voltage with the tip deflection angle increasing exponentially with applied bias until pull-in is reached. The tip deflection changes until the cantilevers bend about 1/3 of the way to the substrate, and if the voltage is increased beyond this point, pull-in occurs, with the cantilevers touching the substrate [45].



(a)



(b)

Figure 7.13. (a) Schematic diagram of the set-up used to calibrate the charge sensors externally, and (b) the tip defection angle as a function of the applied bias between the polysilicon and the substrate for various sizes of paddles, with both the measured and the simulated data shown.

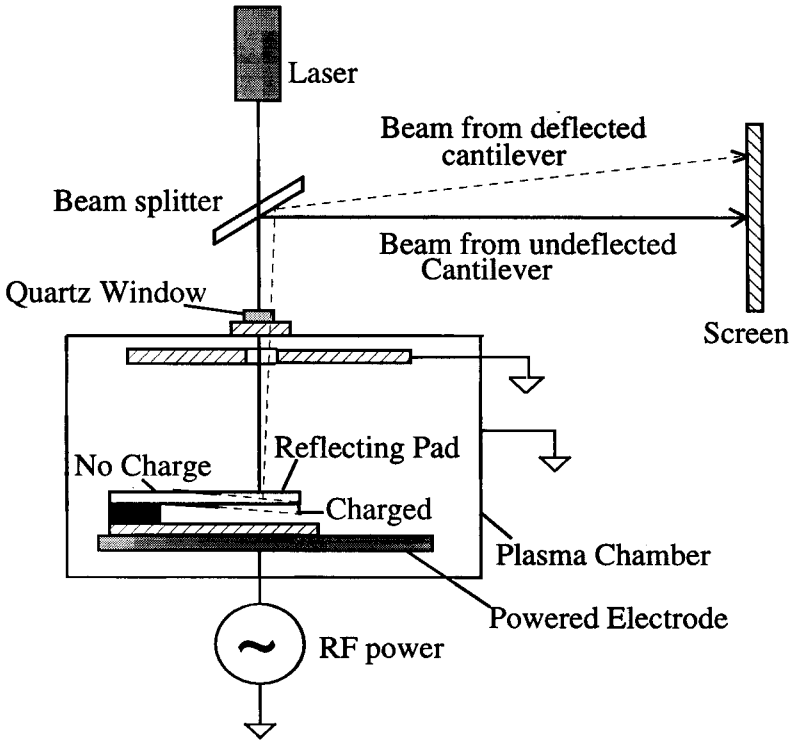


Figure 7.14. Schematic illustration of the set-up used to detect plasma induced charging on the surface directly and non-invasively through measurement of the shift in the laser reflected spot.

Simulations of deflection vs. voltage were performed by the finite difference modeling as described previously in Section 7.2.2. The results are in good agreement with measured data (Fig. 7.13(b)).

Plasma charging measurement

The schematic of the experimental set-up used to detect charging in-situ in the parallel-plate reactor is shown above in Fig. 7.14. A He-Ne laser is directed into the reactor chamber through a quartz window after passing through a beam-splitter. The laser beam covers several identical paddles with similar pull-in voltages so no focusing is necessary. The reflected light is projected onto a screen. When charging occurs, the paddles deflect leading to a shift in the reflected laser spot on the screen. From the tip deflection angle, which can be easily computed from this shift, the charging voltage in

the plasma can be determined. The advantage of this technique is that it is direct and gives accurate results (<5% error). However, the disadvantage is that it requires an optical port and one cannot measure charging voltage at different parts of the electrode.

During plasma exposure, cantilevers that deflect far enough suffer "pull-in" [45] and touch the substrate. When this occurs they often suffer from "stiction", i.e. they remain stuck after the removal of the charge. This can be quickly detected by external inspection under an optical microscope after the plasma exposure. The charging voltage can be estimated by having a range of paddle sizes with different pull-in voltages on the wafer, and observing which ones have pulled-in. Charging voltages inferred by this approach agree well with those measured directly in-situ (Fig. 7.15). The large error bars in case of the ex-situ measurement are due to the difference in pull-in voltages of the different paddles. With this technique, we can only determine the charging voltage to be somewhere between the pull-in voltages of the paddle which was pulled-in and one which was not during the plasma exposure. The main advantage of this method is that no optical ports are required and one can quickly map charging nonuniformities across the electrode. The charge sensors are reusable and the stuck cantilevers can be released by soaking the sample in isopropyl alcohol and drying the sample on the hot plate, as described earlier in Section 7.3.2.

The charging voltage in a parallel-plate reactive-ion-etching (RIE) reactor has been measured by both techniques. The electrode diameter is 24 cm and spacing between the electrodes is 5 cm. The gases are injected into the chamber through a showerhead in the top electrode. All experiments were done in oxygen or argon plasma with RF frequency being 13.56 MHz. These gases were chosen as they do not react with or etch the polysilicon cantilevers.

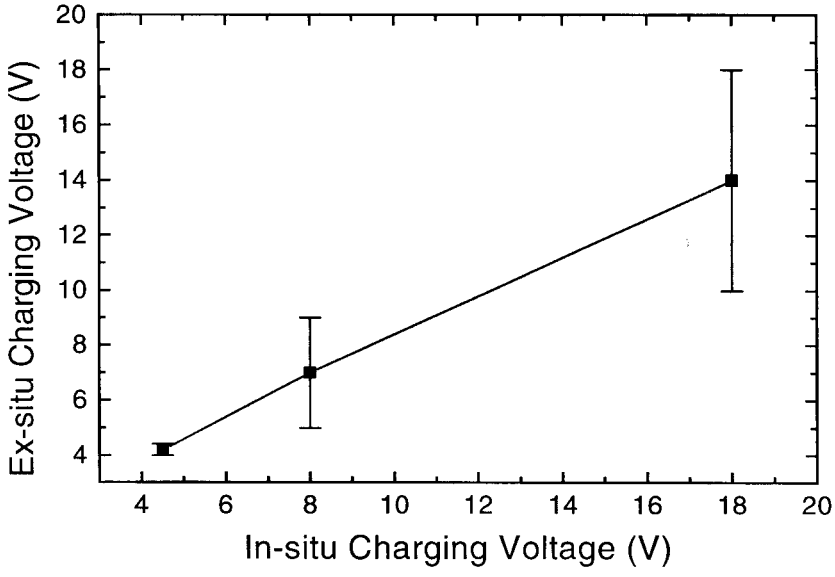


Figure 7.15. Comparison of charging voltage measured by the in-situ direct method (from laser deflection) and that measured by the ex-situ method (from inspecting the paddles after exposure).

The charging voltage near the electrode edge (9.5 cm. from the center) is measured by the in-situ technique. The charging voltage was found to increase as RF input power increased (Fig. 7.16(a)), and charging voltage as large as 20 V was seen. The charging voltage decreased as the chamber pressure was reduced (Fig 7.16(b)), as has been seen by others using electrical probes inside the plasma [19] at the electrode edge, albeit for a different gas. These results clearly demonstrate the utility and versatility of the technique. We also measured charging voltages at the different points on the electrode by the ex-situ method. The charging voltage was lower at the center compared to that at the edge (Fig. 7.17(a)). The charging voltage did not vary much with the flow rate of oxygen (Fig. 7.17(b)). All this data indicates that the charging sensor can be used to choose the plasma parameters leading to least amount charging, so that damage to the actual device during the plasma processing can be minimized.

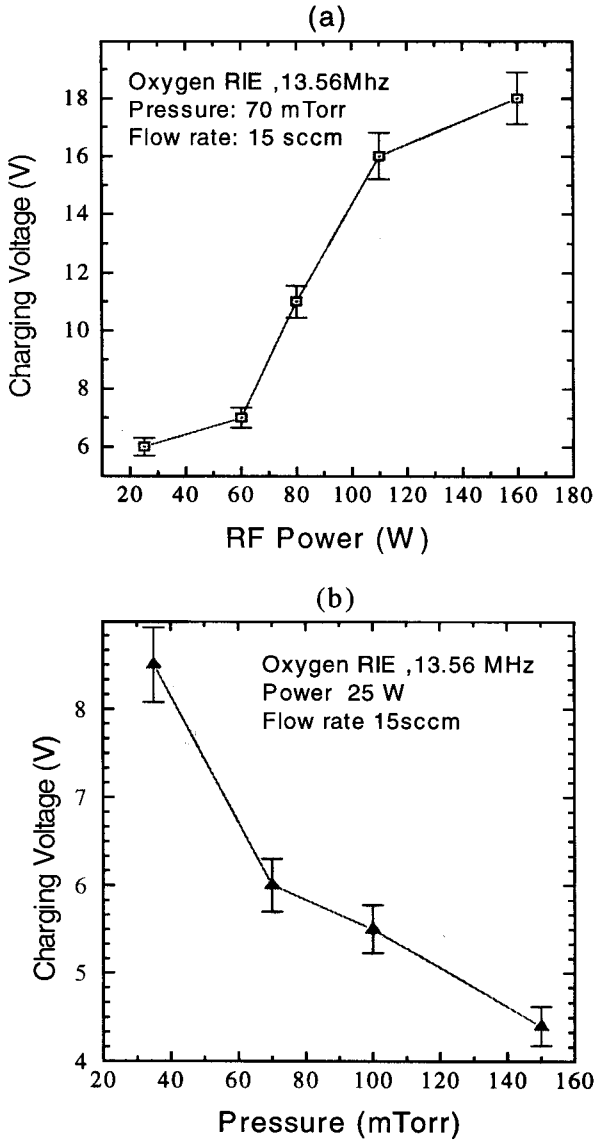


Figure 7.16. (a) Charging voltage as a function of input RF power at constant flow rate and chamber pressure, and (b) charging voltage as a function of chamber pressure at constant flow rate and RF power.

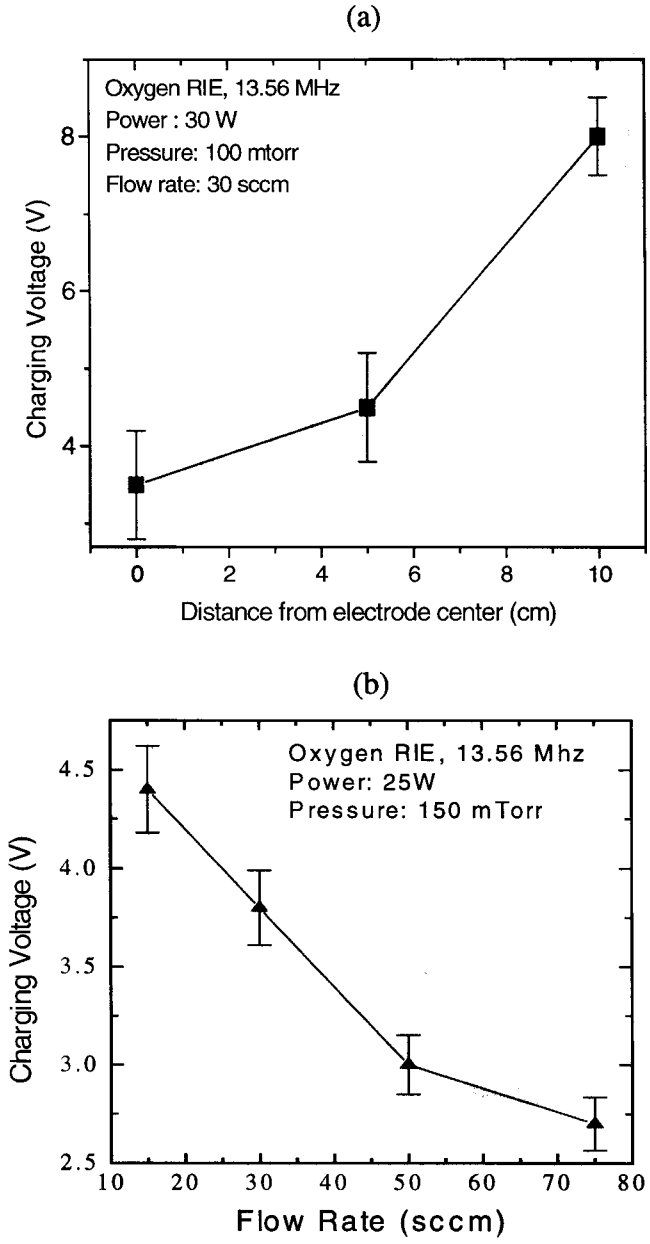


Figure 7.17 (a) Charging voltage as a function position across the electrode at constant RF power, chamber pressure and flow rate, and (b) Charging voltage as a function of flow rate of oxygen gas.

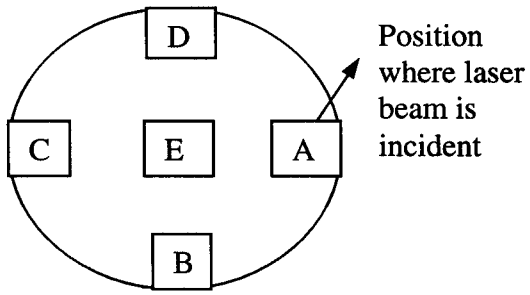


Figure 7.18. Schematic diagram of a 100-mm Si wafer showing the positions of the charge sensors.

In all the experiments above, the sensors were fabricated in 2 cm x 2 cm pieces of Si wafer and placed either directly on the aluminum oxide coated electrode or with a glass slide in between. Another set of experiments was performed with these sensors placed on 100-mm Si wafer at all four particular positions shown in Fig. 7.18. Indium was used to bond the pieces to the Si wafer. The different wafer configurations used are; wafer 1 with sensors placed on Si wafer in contact with the Si and remaining Si not exposed to the plasma (covered with SiO_2), wafer 2 with the sensors placed directly on the Si wafer and the Si wafer exposed to the plasma (no SiO_2), wafer 3 with isolated sensors placed on a Si wafer covered with SiO_2 and Si not exposed to plasma, and wafer 4 with isolated sensors placed on regions of Si wafer with SiO_2 and the remaining Si wafer with no SiO_2 and exposed to the plasma. All the different configurations are shown in Fig. 7.19. The charging voltages as measured by the sensors in the different configurations, were then measured in an O_2 plasma at 60 W, pressure of 150 mtorr and an oxygen flow of 15 sccm. Table 7.2 lists the charging voltage measured at each location for the various configurations.

The charging voltages measured on wafer 1 and wafer 2 are nearly identical indicating that the two configurations are nearly identical from the plasma charging

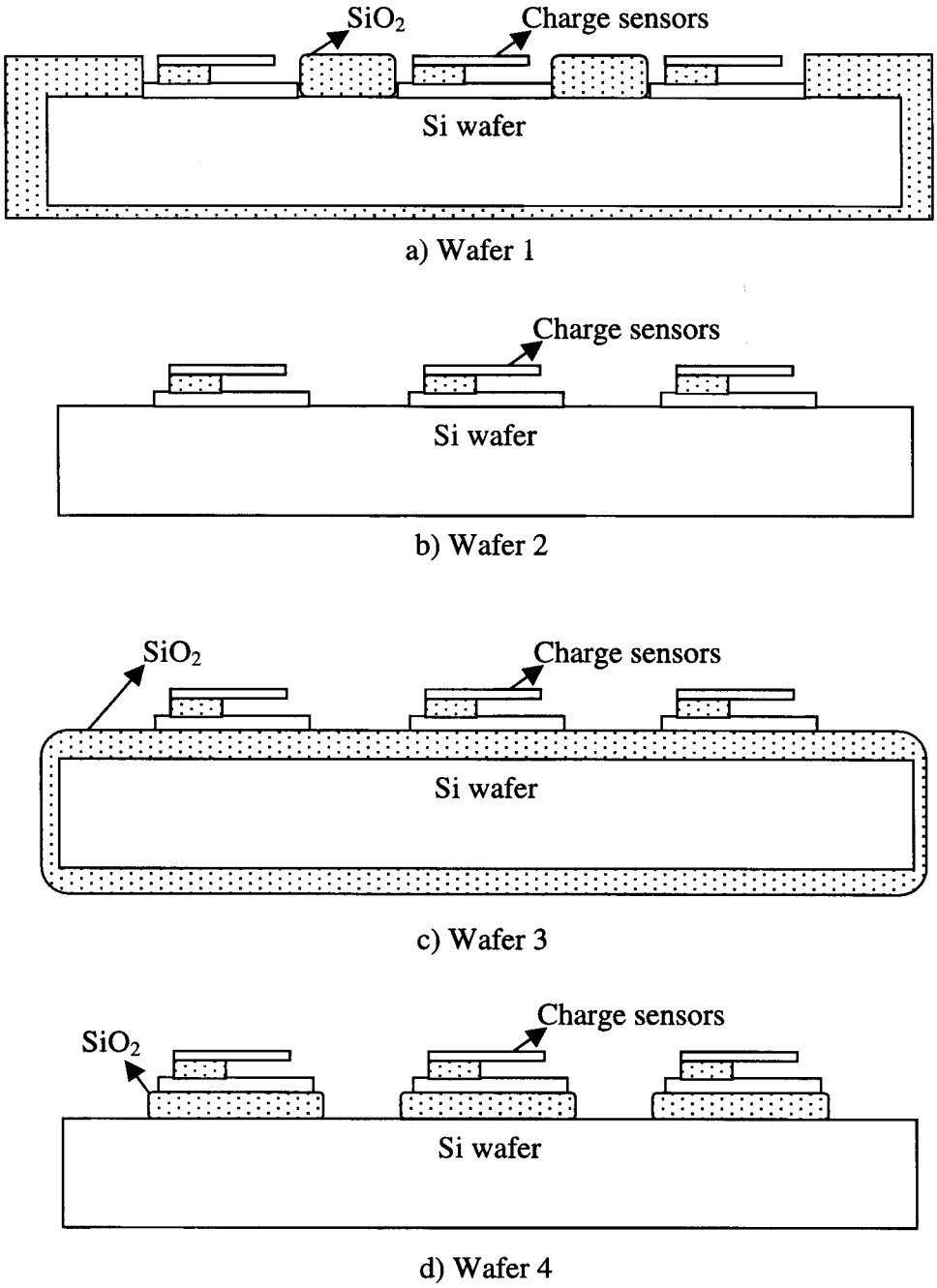


Figure 7.19. Schematic cross-sectional illustrations of the different configurations used to bond the sensors on to the Si wafer to study the charging across a 100-mm Si wafer, when exposed to O_2 plasma at 60 W, pressure of 150 mtorr and an oxygen flow of 15 sccm.

Wafer No.	Charging Voltage measured by sensor (V)				
	Position: A	Position: B	Position :C	Position: D	Position: E
1	8 ± 0.5	5.5 ± 0.5	3.5 ± 0.8	3.8 ± 0.2	4.2 ± 0.2
2	8.5 ± 0.2	5.5 ± 0.5	2.8 ± 0.2	4 ± 0.5	4 ± 0.5
3	6 ± 0.2	5.5 ± 0.5	4.6 ± 0.5	5.2 ± 0.2	5 ± 0.7
4	6.5 ± 0.2	5 ± 0.8	3.5 ± 0.5	4.5 ± 0.5	5 ± 0.5

Table 7.2. The charging voltage for oxygen plasma (60 W, 150 mtorr, and 15 sccm) as measured by sensors on 100-mm Si wafers in the different configurations.

perspective and that the exposure or non-exposure of the Si substrate to the plasma does not matter. In both the cases, for all the sensors the substrate plane was at an equipotential. The charging voltages measured on wafers 3 and 4 are also nearly identical and in both these cases the substrate of each of the sensor was isolated and not at an equipotential. The slight differences in charging voltages between wafer 1 and wafer 3 might be because the substrate is at equipotential in one case while it varies from position to position in the other case. The charging voltage measured is potential difference between the polysilicon cantilever and the substrate, and if the substrate potential changes, the charging voltage changes. This shows that the actual configuration of the wafer during etching plays a crucial role in determining the amount of charging developed.

The charge sensors after fabrication have the same pull-in voltage irrespective of the polarity of the applied gate bias as expected, with the difference in positive and negative pull-in voltage ($\Delta V_{pull\text{-}in}$) less than 0.2 V. However, after plasma exposure $\Delta V_{pull\text{-}in}$ increased to ~1 V. The reason for this increase is not clear. It might be due to charge trapped in the Si_3N_4 layer during the plasma exposure. This change is reversible with the re-release step (soak in isopropyl alcohol and dry on hot plate) resulting in the $\Delta V_{pull\text{-}in}$ voltage to return to the value before the plasma exposure.

To extend the applicability of the charge sensors so that charging in reactive fluorine based plasmas like CF_4, SF_6, CHF_3, CCl_2F_2, etc., can be measured the polysilicon surface was covered with metal like aluminum. This was done by evaporation of thin aluminum after the devices were completely fabricated. The thickness of aluminum has to be less than ~30 nm so that the devices are not shorted. The pull-in voltages of the devices increased after the metal deposition by a factor of two. This could be due to stress created in the polysilicon due to the aluminum layer, as the change of the Young's modulus (E) of the cantilever with the thin aluminum layer is negligible. The effective Young's modulus for the cantilever with multiple layers with different Young's moduli is given by [39]

$$E_{eff} = \frac{E_{Al}t_{Al} + E_{poly-si}t_{poly-Si}}{t_{Al} + t_{poly-Si}} \qquad (7.9)$$

where t's are the thickness of the layers. As $t_{Al} << t_{poly\text{-}Si}$, $E_{eff} \approx E_{poly\text{-}Si}$. These aluminum-coated cantilevers were used to measure charging in CF_4 and Ar plasmas. However, all the paddle structures were stuck after exposure to the plasma. The reason for this is not clear.

7.4 CORRELATION OF SENSOR RESULTS WITH DEVICE DEGRADATION

The extent of plasma charging damage during a particular plasma process depends on the characteristics of the device exposed to the plasma and the configuration of the devices during the exposure. The charge sensors described in the Section 7.2 have a thick dielectric (~2 μm) and the DC current through this device is negligible for the charging voltages we measured. Even at pull-in, the DC current through the device is too small to be measured by the HP 4145 parameter analyzer. However, actual MOS devices have very thin dielectrics (<10 nm) and the I-V characteristics of these devices

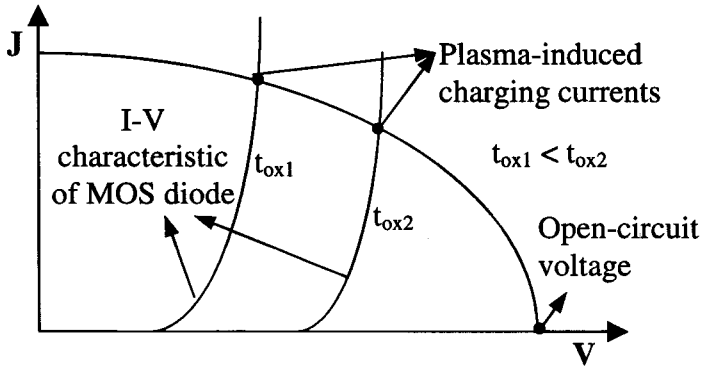


Figure 7.20. Schematic diagram of the J-V characteristics of the charging source and the charging damage seen by MOS devices with different oxide thickness exposed to it [32]. The MEMS charge sensor detects the open-circuit value.

are diode-like with significant DC current passing through the devices at voltages measured by the charge sensors in the plasma. The plasma induced charging has the J-V characteristics as shown in Fig. 7.5 [15] and actual plasma induced voltage across a device depends on the I-V characteristics of the device (Fig. 7.20). The charging voltage measured by the MEMS charge sensor is the open-circuit value, as the sensor does not draw any DC current at these voltages. To check if there is any correlation between the charge sensor reading and actual MOS device damage, MOS capacitors were made and exposed to the plasma under the same conditions [46]. The plasma damage was then quantified by stressing devices externally and comparing the characteristics of the devices with plasma damage and damage due to the external stress.

7.4.1 Fabrication details

MOS capacitors

The MOS capacitors were fabricated on n and p type (100) substrates with 10-30 Ω-cm resistivity (Fig. 7.21). First ~250 nm of field oxide was grown by wet oxidation at 1000 °C after the wafer was cleaned by a partial RCA clean. The RCA clean involved rinsing in H_2O_2 and H_2SO_4 mixture (1:2) for ~10 min and rinsing in DI water and then

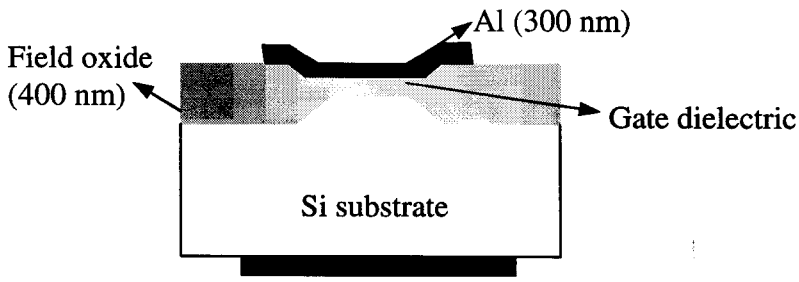


Figure 7.21. Cross-section of the capacitor used in this study, with thermal SiO_2 (8-12.5 nm) as gate dielectric for MOS capacitors and, thermal SiO_2 (~5 nm) and PECVD SiN_x (30-40 nm) as the gate dielectric for the MNOS capacitors.

rinsing in dilute HF before loading in the furnace. The samples were loaded in the furnace with N_2 flowing in the tube and the temperature of the furnace already set to 1000 °C. The samples were annealed in N_2 at the same temperature after the oxidation was complete. Next windows were opened in the field oxide by etching in BHF through patterned photoresist mask. The photoresist was removed by rinsing in acetone and gate oxide of various thickness' (8-12.5 nm) were grown after the partial RCA clean described earlier. The oxidation was done at 850-900 °C with only O_2 flowing in the tube. The samples were annealed after the oxidation in N_2 at the same temperature for ~20 min. In some cases, the samples had a 200-nm thick p^+ polysilicon gate in situ doped with boron ($>10^{20}$ cm^{-3}) grown at 700 °C by rapid thermal chemical vapor deposition (RTCVD). After the gate oxidation (or in some cases, the polysilicon deposition), ~300 nm of aluminum was thermally evaporated and then patterned by wet etching in H_3PO_4 at 65 °C. For the capacitors with polysilicon gate, the aluminum gate with the photoresist on top acts as the mask for the wet etching of polysilicon with a mixture of HNO_3, HF and CH_3COOH. Finally, the capacitors were annealed at 400 °C in forming gas for 30 min. In most cases, the ratio of area of metal on the field oxide to

that on the gate oxide (antenna ratio) was about 0.42. Capacitors with different areas, different perimeter lengths and different antenna ratios were also fabricated (Fig. 7.21).

MNOS capacitors

Metal-nitride-oxide-silicon (MNOS) capacitors with both SiN_x and SiO_2 as the dielectric were also fabricated to quantify the plasma-induced charging damage (Fig. 7.21). Due to different current carrying capabilities of the SiN_x and SiO_2, there will be charge trapped at the SiO_2/SiN_x interface when a charging voltage is applied to the gate of the capacitor [47]. The amount of charge can then be estimated by the flat-band voltage shift in the high frequency C-V curve. The capacitors were fabricated with a process sequence similar to that used for the MOS capacitors, except that gate dielectric was thin SiN_x (30-40 nm) deposited by PECVD at 250 °C using 110 sccm of SiH_4, 25 sccm of N_2 and 35 sccm of NH_3, and chamber pressure of 900 mtorr, on top of thin SiO_2 (~5 nm) grown thermally at 850 °C in O_2. These capacitors had aluminum gates. Aluminum was also evaporated on the backside of the samples to realize the substrate contact. The capacitors were annealed in forming gas at 400 °C prior to testing.

7.4.2 Plasma damage measurement

The plasma damage to the MOS or MNOS capacitors was estimated from the change in the C-V characteristics of the devices. The plasma damage was also simulated by externally stressing the devices and comparing the C-V curves. C-V data plays an important role in all this and in the next section we will described how the measurement is done and how the various parameters like flat-band voltage, interface-state density, are extracted from the C-V data.

C-V measurement

The high frequency (1 MHz) capacitance as a function of the DC applied bias (C-V) was measured with a HP 4275A multi-frequency LCR meter. The probe station

was covered during measurement and coaxial wires were used to minimize noise. The voltage bias was swept from inversion to accumulation of the MOS capacitor. To avoid deep depletion effects, the light was turned on at inversion before the measurement was started. The low frequency C-V was measured by measuring the displacement current across the capacitor for varying DC applied voltage (ramp rate of 1 V/s). This measurement was done on HP 4140B pA meter/DC voltage source. In all cases, the bias was applied to the gate and the substrate was grounded.

In the succeeding analysis, all the capacitance values are capacitance/cm^2. We have for the high-frequency data, $C_{acc}=C_{ox}$ and

$$C_{inv} = \frac{C_s C_{ox}}{C_s + C_{ox}} \qquad (7.10)$$

where C_s is the silicon substrate capacitance and C_{ox} is the oxide capacitance. Rewriting equation (7.10), we have [48]

$$C_s = \left[\frac{1}{C_{inv}} - \frac{1}{C_{ox}}\right]^{-1} = \frac{\varepsilon_s \varepsilon_o}{w_{\max}} \qquad (7.11)$$

$$w_{\max}^2 = \frac{2\varepsilon_s \varepsilon_o \psi_L}{qN_{sub}} \qquad (7.12)$$

$$\psi_L = 2.1\ln\left(\frac{N_{sub}}{n_i}\right) + 2.08 \qquad (7.13)$$

where w_{max} is the maximum depletion region width in the Si substrate, ψ_L is the band-bending at strong inversion, N_{sub} is the Si substrate doping, ε_s is the dielectric constant of Si, and ε_o is the permittivity of free-space. From equations (7.11), (7.12) and (7.13) we have

$$N_{sub} = \left[\frac{2\varepsilon_s \varepsilon_o}{q w_{\max}^2}\right]\left\{2.1\ln\left(\frac{N_{sub}}{n_i}\right) + 2.08\right\} \qquad (7.14)$$

The substrate doping (for uniform doping in the Si wafer) can be determined by iteratively solving equation (7.14). The flat-band silicon capacitance can be determined for uniform doping as [48]

$$C_{FBS} = \frac{\varepsilon_s \varepsilon_o}{\left[\frac{kT\varepsilon_s\varepsilon_o}{q^2 N_{sub}}\right]^{\frac{1}{2}}} \qquad (7.15)$$

and the net flat-band capacitance is given by

$$C_{fb} = \frac{C_{FBS} C_{ox}}{C_{FBS} + C_{ox}} \qquad (7.16)$$

The flat-band voltage was then determined from the high frequency C-V curve for the flat-band capacitance calculated from equation (7.16). The interface-state capacitance (C_{it}) was calculated from the difference between the high (C_{HF}) and low frequency (C_{LF}) capacitance at different gate bias as [48]

$$C_{it}(V_G) = \left[\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right]^{-1} \qquad (7.17)$$

and $C_{it}(\psi_s) = qD_{it}(\psi_s)$, where V_G is the applied gate bias and D_{it} is the interface-state density in $cm^{-2}eV^{-1}$. To determine the interface-state density as a function of energy in the bandgap of silicon we need also to determine ψ_s vs. V_G, and this is calculated from the low frequency C-V plot as [48]

$$\psi_s = \int_{V_{fb}}^{V_G} dV_g \left[1 - \frac{C_{LF}(V_g)}{C_{ox}}\right] \qquad (7.18)$$

From equations (7.17) and (7.18) the interface-state in the bandgap of silicon can then be calculated.

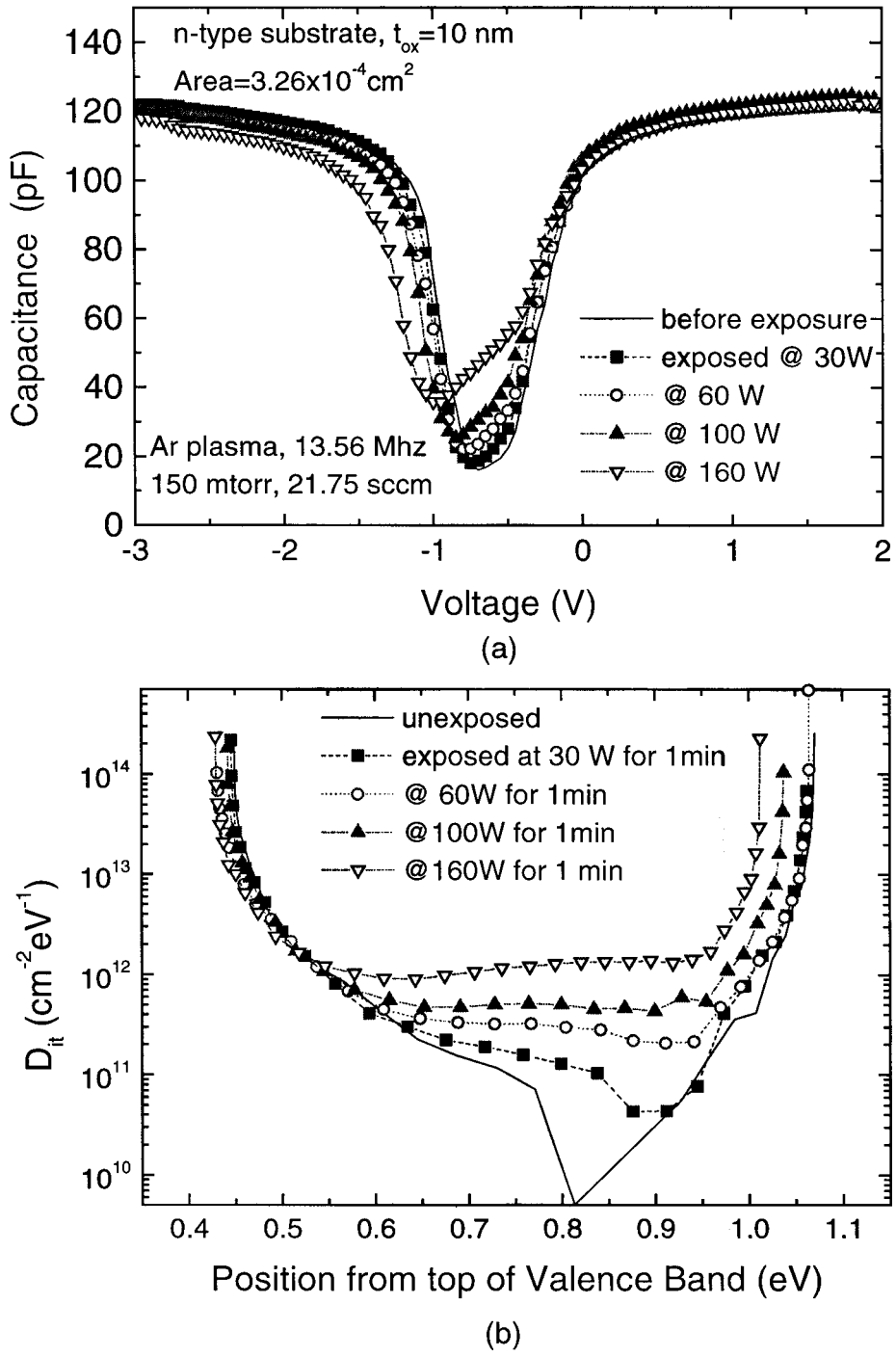


Figure 7.22. (a) Quasi-static C-V curves of MOS capacitors exposed to argon plasma at varying rf powers for 1 min, (b) corresponding interface-state density as a function of position in the band gap.

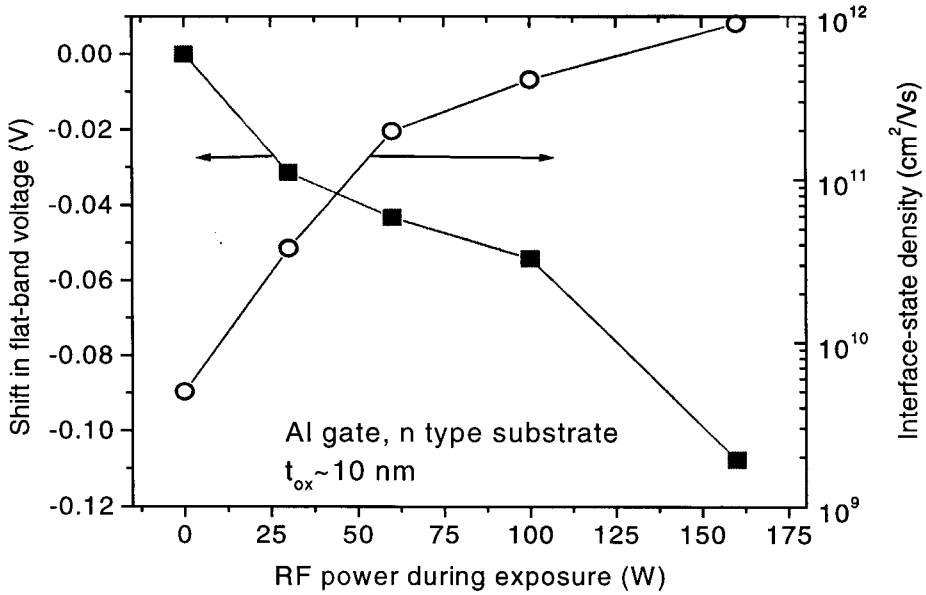


Figure 7.23. Shift in flat-band voltage and change in interface-state density of MOS capacitors after argon plasma exposure at different RF powers.

Results of plasma exposure

We then exposed the MOS capacitors to plasma, varying the RF power, time of exposure and the chamber pressure. The quasi-static (QS) capacitance vs. voltage (C-V) and high frequency C-V was measured after a fixed interval of time (14 min.). The QS C-V curve reflected the degradation of the gate oxide and this degradation scaled with the sensor reading. Fig. 7.22(a) shows the QS C-V curves of various devices exposed to Argon plasma at different RF powers for 1 min and Fig. 7.22(b) shows the corresponding interface-state density, clearly showing that the degradation of gate oxide scales with rf power. Fig. 7.23 shows the change in the flat-band voltage and the change in interface-state density of the MOS capacitors extracted from the high frequency and QS C-V as a function of the plasma RF power during exposure. The flat-band voltage

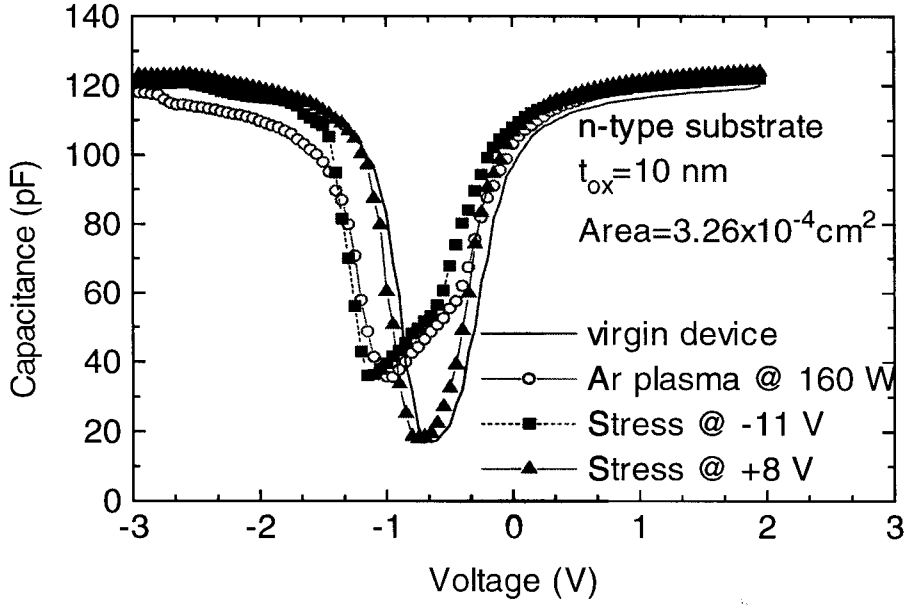


Figure 7.24. Comparison of QS C-V curves of devices exposed to argon plasma at RF power of 160 W and DC bias stressed externally for the same duration.

shift is negative indicating presence of trapped positive charge in the SiO_2 after the plasma treatment.

As reported in earlier work by others [49], we matched the plasma-induced damage with that caused by DC bias stressing of the MOS capacitors. By varying the DC stress, we could estimate the electrical voltage on the gate during the plasma exposure by comparing QS C-V curves. We found that negative bias stress on the gate gave a QS C-V curve that most closely resembled that measured after plasma exposure (Fig. 7.24). Similar results were found for MOS capacitors with p-type substrates, and the plasma-induced voltage increased with oxide thickness [32, 49, 50] (Fig. 7.25). The increase in the charging voltage for thicker oxide is because the thicker oxides turn on (rapid increase in current through the oxide) at higher voltages. Therefore, for the same amount of current density through the oxide, the voltage across

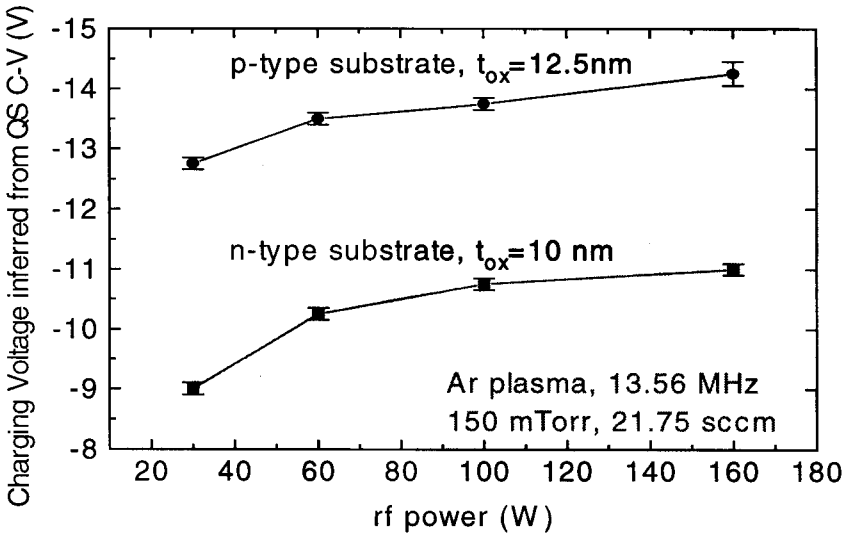


Figure 7.25. Charging voltage across the oxide during argon plasma exposure inferred from DC bias stressing and matching the QS C-V curves for n & p type substrate MOS capacitors.

the thicker oxide will be greater than the potential across the thinner oxide (Fig. 7.13) [32]. This illustrates that the actual plasma damage depends on the characteristics of the device exposed to the plasma. A comparison of the charging voltage as measured by the sensors at different plasma RF power and that inferred from the MOS capacitors is shown in Fig. 7.26. There is a direct one-to-one relation between the two measurements.

MNOS capacitors were also exposed to the plasma and the flat-band voltage shift (ΔV_{fb}) was determined from the high frequency C-V measurement (Fig. 7.27(a)). Fig. 7.27 shows that the flat-band voltage shift due to exposure to argon plasma is much greater than ΔV_{fb} due to oxygen plasma exposure for the same conditions. The charging voltage as measured by charge sensors mirrors this trend with argon plasma having larger charging voltage compared to oxygen plasma (Fig. 7.27(b)). The capacitors were also externally stressed for the same time and the shift in C-V was measured. The plasma induced charging voltage was then estimated from trying to match the high

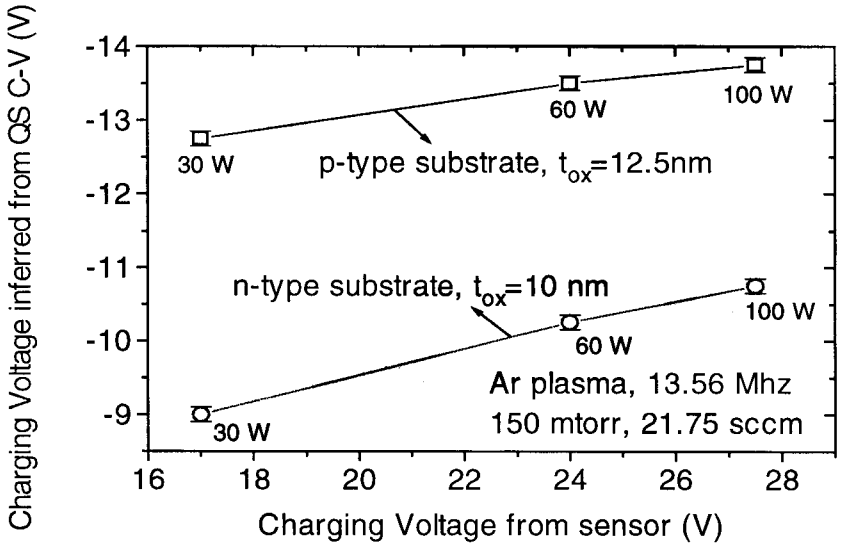


Figure 7.26. Comparison of charging voltage as measured by sensor and inferred from QS C-V degradation at different RF power.

frequency C-V curves. However, it was found that the C-V curves shifted during the measurement itself as the voltages used in measuring the C-V curves resulted in considerable stressing of the capacitors. This might be due to the high number of traps in PECVD SiN_x layer. Hence, estimating the DC bias stress during the plasma treatment from these MNOS capacitors with the PECVD-SiN_x was difficult. Better results are expected for SiN_x deposited stoichometrically by low pressure CVD.

All the data indicates that the with the charge sensor reading one can predict if the damage to an actual device will increase or decrease with change in the plasma conditions, even though the sensor reading does not imply that the actual device will see the same charging voltage under the same plasma conditions.

7.4.3 Effect of UV damage

In addition to the plasma-induced charging damage, the MOS devices exposed to plasma can suffer damage due to UV. The plasma could have energetic photons with energies greater than the bandgap of SiO_2 (~8.8 eV), which result in generation of

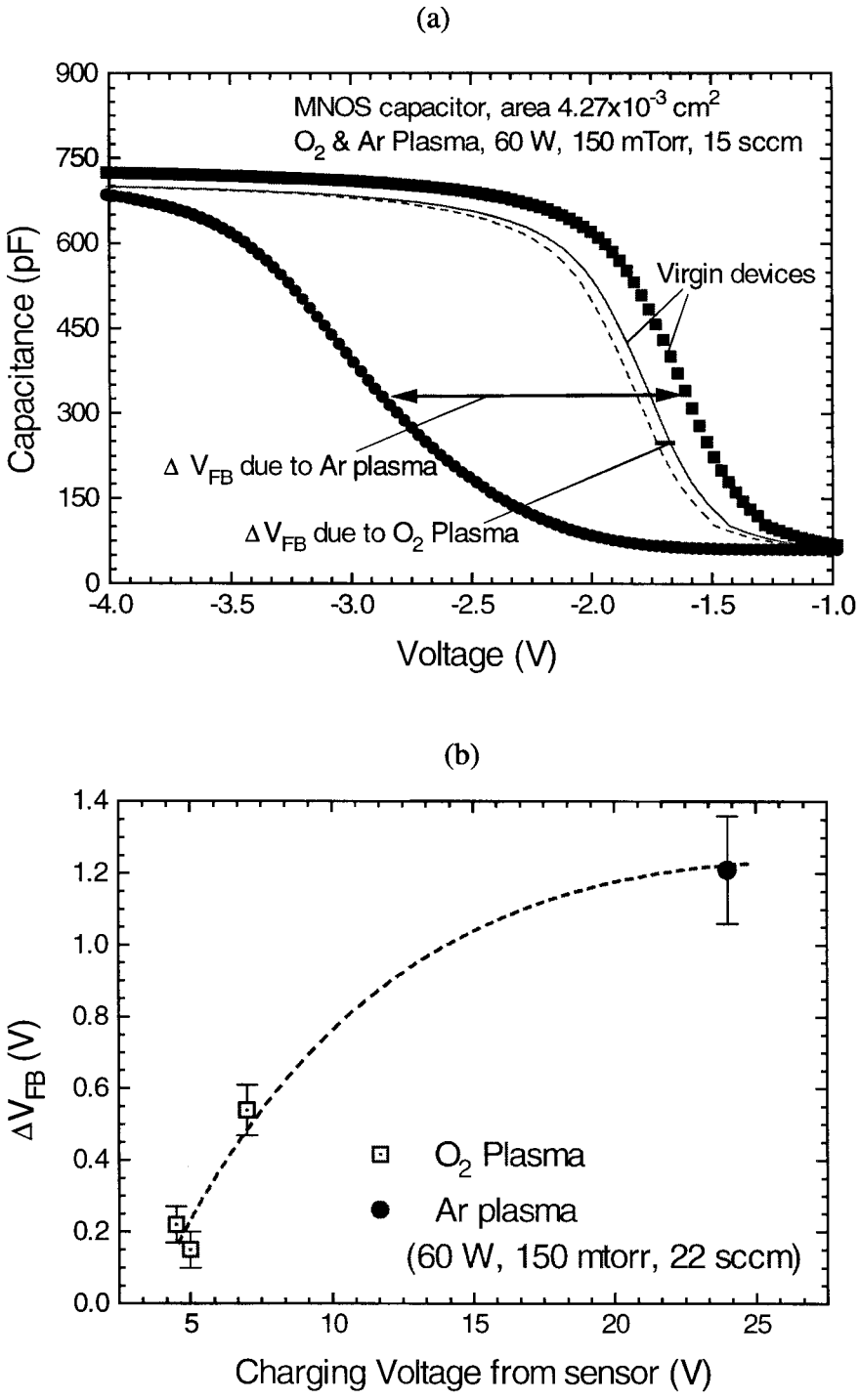


Figure 7.27. (a) High frequency C-V curves of MNOS capacitors before and after exposure to argon and oxygen plasmas. (b) Illustration of the correlation of flat-band voltage shift of MNOS capacitors, after plasma treatment with charge sensor reading.

carriers in the SiO_2 [51]. The DC bias across the oxide and the UV photons-generated carriers can result in significant currents through the oxide and therefore cause damage [51-53]. The typical UV emission in argon plasma occurs at 106.7 and 104.8 nm [51] corresponding to photon energies of 11.6 and 11.8 eV, respectively. The absorption depths in aluminum as determined from the absorption coefficient [54], at these wavelengths are 21.47 and 18.89 nm, respectively. This indicates that aluminum gates about 300 nm thick should effectively block the UV. However, in our work, it was found that aluminum gates do not completely shield the UV.

To confirm that UV also plays a significant role in the plasma damage of the MOS capacitors, MOS capacitors with varying thickness of aluminum gates (37, 110, 250, 700 nm) were fabricated and exposed to argon plasma at 60 W, pressure of 150 mtorr and argon flow rate of 15 sccm. The samples were cut into small pieces and the sides and the substrate of the sample was covered with photoresist to ensure that there is no DC current path from the plasma to the MOS device. The thickness of the gate oxide in all cases was ~75 nm. The exposure time was 2 min and the degradation of the quasi-static C-V was measured in all cases (Fig. 7.28(a)). However, the capacitors with poly-Si gates showed practically no degradation in quasi-static C-V indicating that, poly-Si and aluminum gate blocks UV more effectively than only aluminum gate (Fig. 7.28(b)). This is because poly-Si is essentially opaque to photons with energies between 3 to 20 eV [55] and aluminum is opaque to photons with energies >20 eV, so with capacitors with aluminum and poly-Si as the gate, nearly all the high-energy photons are blocked. In these experiments the damage from charging damage cannot be discounted as the UV creates carriers in the oxide and the charging voltage results in an electric field across the oxide which separates the carriers generated leading to oxide damage. This illustrates that plasma damage is quite difficult to study and quantify, and each method

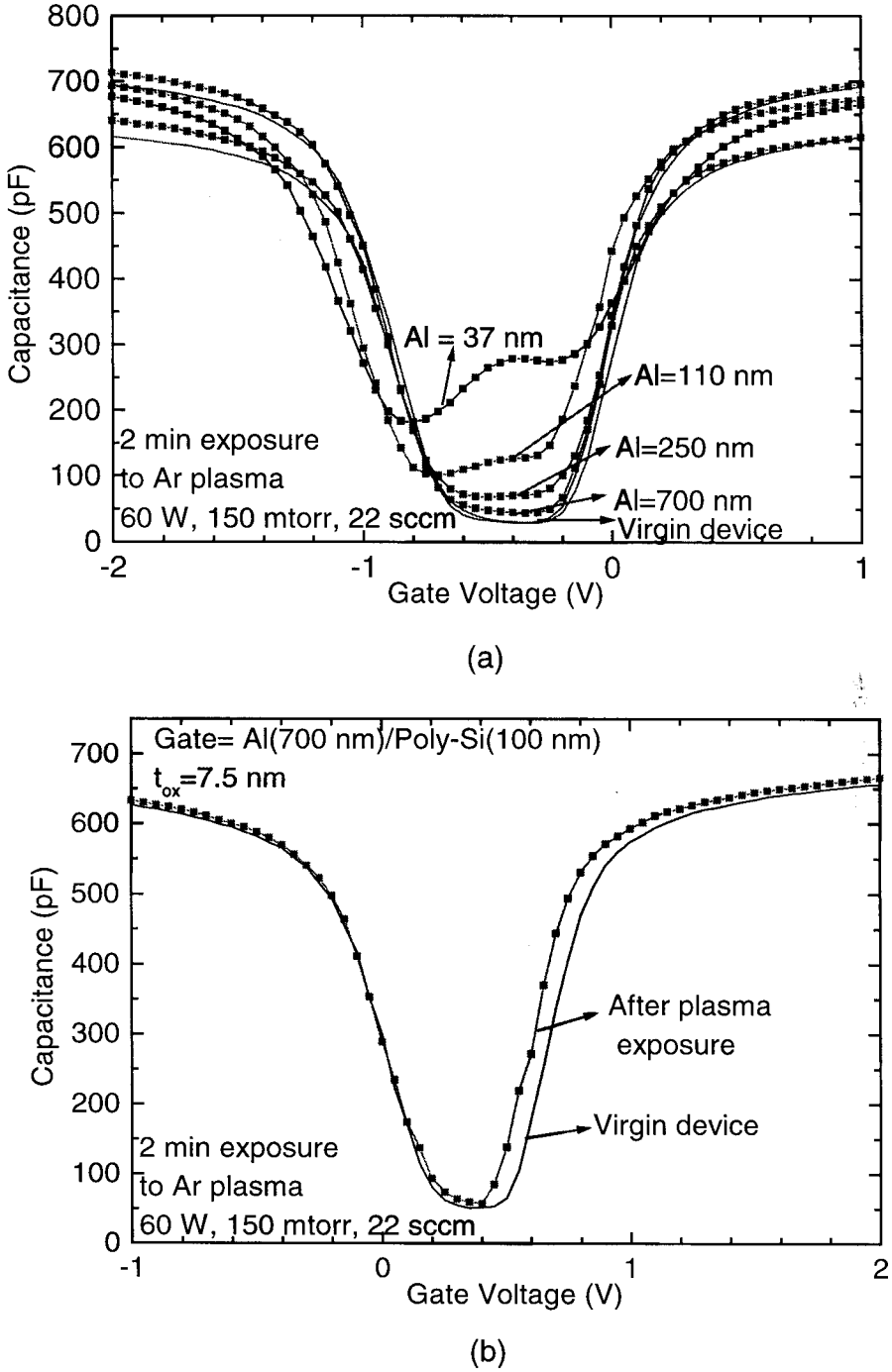


Figure. 7.28. Quasi-static C-V curves before and after exposure to argon plasma for 2 min at 60 W, of (a) MOS capacitors with varying thickness of aluminum gate, and (b) MOS capacitors with aluminum and poly-Si gate.

has its advantages and disadvantages. None of the methods can entirely predict the damage caused to an actual device during plasma processing. In case of the charge sensors, UV does not play any role in the charge sensor reading, and they only quantify the plasma-induced charging at the surface

7.5 SUMMARY AND FUTURE WORK

In summary we have demonstrated a non-invasive method for quickly measuring charging effects which occur in plasma-based semiconductor processing. The method also allows in-situ measurement of the charge or mapping charging effects over large areas. The method should prove valuable for the developments of advanced etch processes, and the structure may prove useful for general charge sensing problems. We have shown that the sensor can be used to predict damage to gate oxides resulting from plasma process. For correlation of actual device deterioration due to plasma exposure to the charge sensor reading, MOS capacitors with poly-Si/aluminum gates fabricated on large 100-mm Si wafer have to be used, to minimize the UV photons effect.

Further work is necessary to extend the charge sensor concept so that the actual device damage can be predicted. One extension is that series of resistors can be added to the structure between the polysilicon cantilever and the substrate so that the plasma charging current vs. charging voltage can be effectively mapped (similar to the CHARM-2 sensor). Right now, the sensor only measures the open-circuit charging voltage. Once charge sensors with variable current vs. applied voltage characteristics are made, increasing the polysilicon area on the support vis-à-vis the polysilicon area that deflects can easily incorporate the antenna effect, where a large charge collecting region is connected to region sensitive to the charge.

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Chapter 8

CONCLUSION

8.1 SUMMARY

We started our work studying the plasma-seeding technique so the nucleation in *a*-Si films and therefore the grain boundary locations in the final polysilicon films can be controlled. We found that room-temperature RF hydrogen plasma treatment of thin hydrogenated amorphous silicon (*a*-Si:H) films deposited by plasma-enhanced chemical vapor deposition resulted in reduction of subsequent crystallization time of the films. This effect could also be controlled so that only certain regions of the films are seeded, thereby giving us the tool by which grain boundary locations in polysilicon films could be controlled. We studied this plasma-enhancement effect to understand the mechanism and its effect on the structural and electrical properties of the polysilicon films. We believe that exposure to hydrogen plasma leads to hydrogen abstraction from the surface of the *a*-Si:H films leading to creating of Si dangling bonds. This facilitates the formation of crystalline Si-Si bonds. These crystalline Si nuclei are passivated by hydrogen creating $Si-H_2$ at the ends leading to the characteristic IR peak at 2100 cm^{-1} after plasma treatment. The nuclei are formed at the top 30-40 nm of the surface. During the subsequent anneal, these nuclei grow leading to complete crystallization of the films in shorter times.

In the second part of our work, we studied the electrical properties of these plasma-treated polysilicon films and fabricated n-channel self-aligned TFTs in them using both high-temperature thermally grown gate oxide and PECVD oxide. We then studied in detail the effect of reduced crystallization time on the characteristics of the TFTs and determined that field-effect mobility increases when grain size of the films are of the order of the channel length. We also found that the gate oxide plays an important role in determining the subthreshold slope and leakage current of the TFTs.

We then used the plasma-seeding technique to control grain boundaries locations and thereby fabricate transistors with higher mobility by selectively seeding the source and drain regions of the transistor. Subsequent anneal led to lateral crystallization from the seeded source/drain regions into the channel leading to larger grains. We studied this process in detail, studying the effects of annealing temperature and time, processing sequence, and growth temperature of precursor *a*-Si:H films.

Selective seeding also meant that by masking the *a*-Si:H films during the plasma treatment, polycrystalline and amorphous regions could be realized on the same substrate. However, the key issue to fabricate TFTs in the two regions was the loss of hydrogen from the amorphous regions during the 600 °C selective crystallization anneal, which meant that the amorphous Si was no longer device quality. We successfully put the hydrogen back into the film to fabricate top-gate non-self-aligned TFTs in both the amorphous and polycrystalline regions. All processing steps to fabricate the *a*-Si:H and poly-Si TFTs were shared. This technology is of tremendous importance in the AMLCD business, for the integration of row/column driver circuits (poly-Si TFTs) and pixel switching TFTs (*a*-Si:H TFTs) on the same substrate to keep costs down.

We also developed a non-invasive, in-situ and direct method to quantify the amount of surface charging during plasma exposure. The method relied on the fact a cantilever acts as a deflectable capacitor and any charging of the cantilever surface leads to deflection of the cantilever, which can be detected using a laser beam.

8.2 FUTURE WORK

As we had discussed in chapter 6, we have still not reached the goal of obtaining single-crystal Si layers on insulating substrates at low temperatures. The intra-grain defects in the silicon layers after SPC have to be minimized without resorting to high-temperature anneal. The grain orientation both vertical and in-plane needs to be controlled so as to realize (100) surfaces. In chapter 6, we made some suggestions on how these issues might be tackled.

In addition, better understanding of the hydrogen-plasma-seeding mechanism is needed. The crystallite-formation kinetics during hydrogen plasma treatment has to be studied. The size of these crystallites, their distribution in the *a*-Si:H films and the orientation of the crystallites also needs to be investigated. Also, the effect of the deposition conditions (like PECVD vs. LPCVD) of the amorphous films on the subsequent crystallite formation during hydrogen plasma treatment needs to be thoroughly examined. LPCVD might be the preferred growth technique so as to minimize contamination, from O, C, N, etc during growth, in the amorphous films. The effect of other sources of hydrogen ions (like during ion implantation, or ion-shower doping) on the crystallite formation needs to be studied.

In our work we opened 4-μm holes in the SiO_2 mask and exposed the sample to hydrogen plasma, to create several seed nuclei in each hole. Towards the goal of

obtaining single grains at predetermined locations in the Si films, the effect of size of mask on number of seed nuclei created in each hole should be investigated.

Finally, from the devices standpoint, p-channel transistors and later CMOS circuits need to be fabricated. The work of integrated *a*-Si:H and poly-Si TFTs can also be extended, and self-aligned TFTs fabricated to achieve better performance. As discussed previously in Section 5.4.3, a self-aligned process was not used in integrated TFT fabrication due to the additional high-temperature anneal required to activate the dopants after the source/drain implant leading to further loss of hydrogen from the amorphous regions. However, others have shown that hydrogen implantation along with or after the dopant implantation [1], or the use of hydrogen in ion shower doping [2], eliminates the need for any high-temperature anneal. We should investigate this further to fabricate self-aligned integrated *a*-Si:H and poly-Si TFTs.

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Appendix A

GROWTH RECIPES IN S900 MULTI-CHAMBER PECVD SYSTEM

A.1 UNDOPED AMORPHOUS SILICON (I-CHAMBER)

1) 150 nm *a*-Si:H at 150 °C at RF power ~4.5 W (net): aSi150a.rcp

Step No.	Description	Time (s)	DC Power (mA)	Pressure (mtorr)	Set point temperature (°C)			Flow rate (sccm)		
					Heater 1	Heater 2	Heater 3	Ar	H_2	SiH_4
1	Ar flush	60		650	150	150	130	50		
2	H_2 flush	120		650	"	"	"		50	
3	H_2 plasma	120	75	650	"	"	"		50	
4	H_2 flush	120		500	"	"	"		50	
5	SiH_4 flush	120		500	"	"	"			50
6	Si dep.	1000		500	"	"	"			50
7	SiH_4 flush	120		500	"	"	"			50
8	Ar flush	120		500	"	"	"	50		

2) 150 nm *a*-Si:H at 250 °C at RF power ~4.5 W (net): aSi250.rcp

Step No.	Description	Time (s)	DC Power (mA)	Pressure (mtorr)	Set point temperature (°C)			Flow rate (sccm)		
					Heater 1	Heater 2	Heater 3	Ar	H_2	SiH_4
1	Ar flush	60		650	250	250	230	50		
2	H_2 flush	120		650	"	"	"		50	
3	H_2 plasma	120	75	650	"	"	"		50	
4	H_2 flush	120		500	"	"	"		50	
5	SiH_4 flush	120		500	"	"	"			50
6	Si dep.	1000		500	"	"	"			50
7	SiH_4 flush	120		500	"	"	"			50
8	Ar flush	120		500	"	"	"	50		

3) 150 nm *a*-Si:H at 350 °C at RF power ~4.5 W (net): aSi350.rcp

Step No.	Description	Time (s)	DC Power (mA)	Pressure (mtorr)	Set point temperature (°C)			Flow rate (sccm)		
					Heater 1	Heater 2	Heater 3	Ar	H_2	SiH_4
1	Ar flush	60		650	350	350	340	50		
2	H_2 flush	120		650	"	"	"		50	
3	H_2 plasma	120	75	650	"	"	"		50	
4	H_2 flush	120		500	"	"	"		50	
5	SiH_4 flush	120		500	"	"	"			50
6	Si dep.	1000		500	"	"	"			50
7	SiH_4 flush	120		500	"	"	"			50
8	Ar flush	120		500	"	"	"	50		

A.2 DOPED AMORPHOUS/MICROCRYSTALLINE SILICON (P-CHAMBER)

1) 250 nm n^+ *a*-Si:H at 300 °C, RF power ~4.5 W (net): naSi2k6b.rcp

Step No.	Description	Time (s)	Pressure (mtorr)	DC power (mA)	Set point temperature (°C)			Flow rate (sccm)		
					Heater 1	Heater 2	Heater 3	Ar	SiH_4	PH_3
1	Ar flush	120	500		300	300	300	50		
2	SiH_4 flush	120	500		"	"	"		50	
3	PH_3 flush	120	500		"	"	"		44	6
4	n-aSi dep.	1500	500		"	"	"		44	6
5	n-aSi flush	120	500		"	"	"		44	6
7	SiH_4 fush	60	500		"	"	"		50	
8	Ar Flush	120	500		"	"	"	50		

2) 50-60 nm n^+ μc-Si:H at ~340 °C, RF power ~75 W (net): nmcSi0k7.rcp

Step No.	Description	Time (s)	Pressure (mtorr)	DC power (mA)	Set point temperature (°C)			Flow rate (sccm)			
					Heater 1	Heater 2	Heater 3	Ar	H_2 Dil.	SiH_4	PH_3
1	H_2 flush	20	500		350	350	340		7		
2	H_2 flush	30	900		"	"	"		41		
3	H_2 flush	60	500		"	"	"		100		
4	SiH_4 flush	30	500		"	"	"		100	2	
5	PH_3 flush	30	500		"	"	"		100	2	6
6	PH_3 flush	180	500		"	"	"		100	2	12
7	nmcSi dep.	1000	500		"	"	"		100	2	12
8	PH_3 flush	180	500		"	"	"		100	2	12
9	Ar flush	120	500		"	"	"	50			

A.3 SILICON NITRIDE (N-CHAMBER)

1) 150 nm *a*-SiN_x:H at 200 °C at RF power ~20 W (net): SiN3_1k5.rcp

Step No.	Description	Time (s)	Pressure (mtorr)	DC power (mA)	Set point temperature (°C)			Flow rate (sccm)			
					Heater 1	Heater 2	Heater 3	Ar	H_2 Dil.	SiH_4	NH_3
1	Ar flush	120	500		200	200	200	50			
2	H_2 flush	60	500		"	"	"		5		
3	H_2 flush	60	500		"	"	"		50		
4	H_2 flush	60	500		"	"	"		220		
5	SiH_4 flush	60	500		"	"	"		220	5	
6	NH_3 flush	120	500		"	"	"		220	5	50
7	SiN_x dep.	1200	500		"	"	"		220	5	50
8	NH_3 flush	120	500		"	"	"		220	5	50
9	Ar Flush	120	500		"	"	"	50			

2) 150 nm *a*-SiN_x:H at 300 °C at RF power ~5 W (net): SiN2_1k5.rcp

Step No.	Description	Time (s)	Pressure (mtorr)	DC power (mA)	Set point temperature (°C)			Flow rate (sccm)			
					Heater 1	Heater 2	Heater 3	Ar	H_2 Dil.	SiH_4	NH_3
1	Ar flush	120	500		300	300	300	50			
2	H_2 flush	60	900		"	"	"		10		
3	H_2 flush	60	500		"	"	"		75		
4	H_2 flush	60	500		"	"	"		143		
5	SiH_4 flush	60	500		"	"	"		143	13	
6	NH_3 flush	120	500		"	"	"		143	13	130
7	SiN_x dep.	1000	500		"	"	"		143	13	130
8	NH_3 flush	120	500		"	"	"		143	13	130
9	Ar Flush	120	500		"	"	"	50			

A.4 HYDROGENATION (I-CHAMBER)

1) Hydrogen plasma passivation of poly-Si transistors at 350 °C at RF power ~135 W (net): H2_60.rcp

Step No.	Description	Time (s)	DC Power (mA)	Pressure (mtorr)	Set point temperature (°C)			Flow rate (sccm)	
					Heater 1	Heater 2	Heater 3	Ar	H_2
1	Ar flush	120		500	350	350	350	50	
2	H_2 flush	120		1000	"	"	"		50
3	H_2 plasma	3600		1000	"	"	"		50
4	H_2 flush	120		1000	"	"	"		50
5	H_2 flush	60		500	"	"	"		50
6	Ar flush	120		500	"	"	"	50	

2) Rehydrogenation of *a*-Si after the high-temperature anneal (integration of *a*-Si:H and poly-Si TFTs) is done after preparation of the chamber and sample holder, i.e. dummy coat of *a*-Si:H.

a) Dummy coat of 360 nm of *a*-Si:H at 150 °C at RF power ~4.5 W (net): aSicoat.rcp

Step No.	Description	Time (s)	DC Power (mA)	Pressure (mtorr)	Set point temperature (°C)			Flow rate (sccm)	
					Heater 1	Heater 2	Heater 3	Ar	SiH_4
1	Ar flush	120		500	150	150	130	50	
2	SiH_4 flush	120		1000	"	"	"		50
3	aSi dep.	2400		1000	"	"	"		50
4	SiH_4 flush	120		1000	"	"	"		50
5	Ar flush	120		500	"	"	"	50	

b) Hydrogen plasma to insert hydrogen in *a*-Si films at 350 °C at RF power ~45 W (net): H2_75.rcp

Step No.	Description	Time (s)	DC Power (mA)	Pressure (mtorr)	Set point temperature (°C)			Flow rate (sccm)	
					Heater 1	Heater 2	Heater 3	Ar	H_2
1	Ar flush	120		500	350	350	350	50	
2	H_2 flush	120		1000	"	"	"		50
3	H_2 plasma	4500		1000	"	"	"		50
4	H_2 flush	120		1000	"	"	"		50
5	H_2 flush	60		500	"	"	"		50
6	Ar flush	120		500	"	"	"	50	

Appendix B

AMORPHOUS SILICON CHARACTERIZATION TECHNIQUES

B.1 INFRARED TRANSMISSION

The infrared (IR) transmission of the samples with *a*-Si:H films deposited on bare p-type lightly doped (~10-50 Ω-cm) Si wafers which were polished on both surfaces, was measured on a Nicolet FTIR setup. Si wafers were used as substrates as glass is not transparent in the IR range. For this work, we needed to determine the hydrogen content in the amorphous films. The net hydrogen content in atomic % (N) in the *a*-Si:H films can be easily determined from the integrated absorption coefficient (α) at 630 cm^{-1} which arises due to wagging modes of Si-H and Si-H_2 bonds [1-3], as

$$N = \frac{2.1x10^{20} cm^{-2}}{5x10^{23} cm^{-3}} \int \frac{\alpha(\omega)}{\omega} d\omega \qquad \text{(B.1)}$$

The absorption coefficient (α) is calculated from the interference-free infrared transmittance (T) data of the films from [3]:

$$T_{total} = T_{film} T_{substrate} \qquad \text{(B.2)}$$

$$T_{film} = \frac{(1-R)^2 e^{-\alpha d}}{1-R^2 e^{-2\alpha d}} \qquad \text{(B.3)}$$

where, α is the absorption coefficient, d the film thickness, T_{film} is the transmittance of the film, and R the reflection loss of the film. We can determine R from

$$R = \frac{(n-1)^2}{(n+1)^2} \qquad \text{(B.4)}$$

where, n is the index of refraction of the film. Equation (B.4), however, ignores the loss from multiple reflections at the film/substrate interface. Equation (B.3) can then be solved for α in terms of measured T_{film}.

B.2 OPTICAL TRANSMISSION AND PHOTO-THERMAL DEFLECTION SPECTROSCOPY

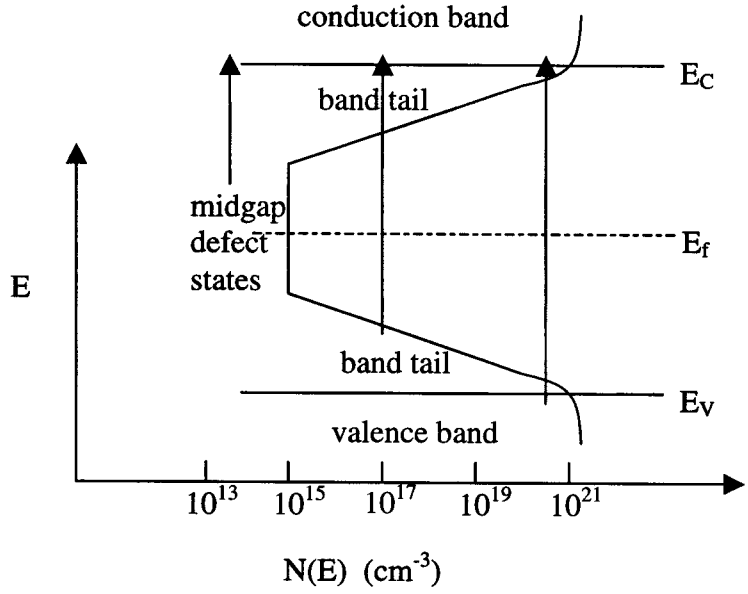

Figure B.1. A schematic density of states diagram. States located between E_C and E_V are localized. States above E_C (in the conduction band) or below E_V (in the valence band) are extended. Arrows show possible optical transitions to the conduction band from midgap states, tail states, or valence band states.

There are some very significant differences in the optical absorption between crystalline and amorphous semiconductors. Three regions may be defined for the absorption of amorphous silicon (Fig. B.1). The lowest energy region (I) corresponds to the transitions from the defect states to the conduction band, or from valence band state into defect states. The transition region (II) in *a*-Si:H, over which the absorption

coefficient increases exponentially by four orders of magnitude represents absorption by "tail states" due to the presence of dangling bonds in the amorphous film [4]. The absorption coefficient has a characteristic slope defined by the equation $\alpha = \alpha_o \exp(E/E_{Urbach})$ and is called the Urbach edge or tail [5]. Beyond the Urbach edge (III) the absorption coefficient increases less quickly, usually as some power law of the energy, and the absorption takes place between the valence and conduction bands, similar to the absorption observed for direct band-to-band transitions in crystalline silicon. Therefore with the measurement of the absorption coefficient for different photon energies, from sub band-gap (~1.0 eV) to above band-gap (~2.0 eV), the defect density in amorphous silicon can be estimated [6].

B.2.1 Optical transmission

To determine the optical absorption (region III) and optical bandgap (Tauc gap), and the thickness of the films, optical transmission of *a*-Si:H films deposited on glass substrates was measured. A Hitachi H-3410 spectrophotometer was used, and the range of wavelengths measured was from 300-2500 nm. A monochromatic light beam is split, and one half is incident on the sample, behind which is the photodetector, while the other half goes directly to another detector to count the number of incident photons. The ratio of the two detector outputs is the transmittance of the sample (Fig. B.2). The absorption coefficient (α) in the strongly-absorbing region, was then determined by deconvoluting the transmission data following the Swanepoel method [7].

The method involves, determining the thickness of the film (d) from the interference fringes in the transmission data as,

$$2n_1 d = m\lambda_1 \qquad \text{(B.5)}$$

and $$2n_2 d = (m+1)\lambda_2 \qquad \text{(B.6)}$$

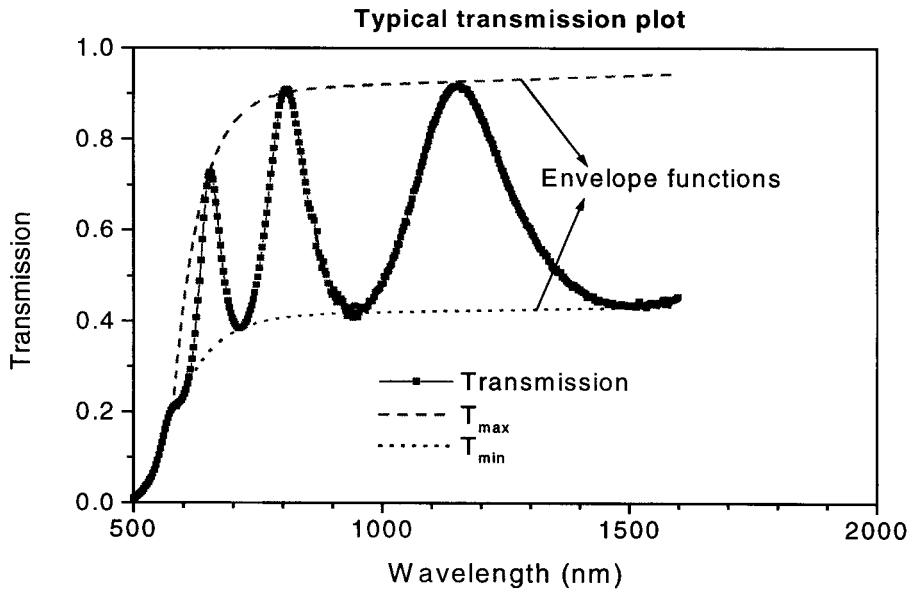

Figure B.2. Transmission of light through a thin film as function of wavelength of light. The maxima and minima occur because of constructive and destructive interference.

for two adjacent maxima or minima (m is the order parameter of the interference and is integral for maxima and half integral for minima), and eliminating m between equations (B.5) and (B.6) and solving for d we find,

$$d = \frac{\lambda_1 \lambda_2}{2(n_2\lambda_1 - n_1\lambda_2)} \qquad \text{(B.7)}$$

To calculate d we need to know the index of refraction at these wavelengths. We note that complete transmission including the interference fringes can be written as [7]

$$T = \frac{Ae^{-\alpha d}}{B - Ce^{-\alpha d}\cos\varphi + De^{-2\alpha d}} \qquad \text{(B.8)}$$

$$\varphi = \frac{4\pi n d}{\lambda} \qquad \text{(B.9)}$$

where T is the transmission, A, B, C, and D are constants depending on the indices of refraction of the substrate and of the film, n is the index of refraction of the film. The maxima and minima of the transmission can then be written by

$$T_{max} = \frac{Ae^{-\alpha d}}{B - Ce^{-\alpha d} + De^{-2\alpha d}} \quad \text{(B.10)}$$

$$T_{min} = \frac{Ae^{-\alpha d}}{B + Ce^{-\alpha d} + De^{-2\alpha d}} \quad \text{(B.11)}$$

Eliminating $e^{-\alpha d}$ between (B.10) and (B.11) we can solve for the index of refraction as

$$n = [M + (M^2 - s^2)^{\frac{1}{2}}]^{\frac{1}{2}} \quad \text{(B.12)}$$

$$M = 2s(\frac{1}{T_{min}} - \frac{1}{T_{max}}) + \frac{s^2 + 1}{2} \quad \text{(B.13)}$$

where s is the index of refraction of the substrate. To obtain n at all wavelengths using the above method, the value of T_{max} and T_{min} for each wavelength is needed. This is estimated by fitting an envelope function of the form: $a–\exp(-b\lambda+c)+d\lambda$, where a, b, c and d are fitting variables to the transmission maxima and minima (Fig. B.2). Once the first approximation to the index of refraction is obtained, the thickness d can be then determined using equation (B.7). With this value of d, the order parameter m can be estimated (closest integer value) and a more accurate value of d can then be recalculated.

In the strongly absorbing region ($\alpha d >> 1$), we can approximate transmission as

$$T \approx \frac{Ae^{-\alpha d}}{B} \quad \text{(B.14)}$$

where $A = 16n^2s$ and $B = (n+1)^3(n+s^2)$. Thus we obtain

$$\alpha = -\frac{\ln(\frac{BT}{A})}{d} \quad \text{(B.15)}$$

We can then determine the Tauc gap (E_{Tauc}) by fitting a straight line to $(\alpha E)^{1/2}$ vs. E plot and obtaining the x-intercept.

B.2.1 Photo-thermal deflection spectroscopy

The optical transmission measurement, however, cannot be used to determine the absorption coefficient with any accuracy when it is very small, i.e. in the weakly absorbing or transparent regions (regions II and I). Therefore other techniques like photo-thermal deflection spectroscopy (PDS) was used to measure small α. This technique involves deflection of a laser beam which just skims the surface of the film. Monochromatic light incident upon the sample is absorbed and excites electrons to higher energy states. When the excited electrons relax they give off heat to the sample and the surrounding fluid (Flourinert FC-72). This causes a gradient in the index of refraction in the fluid next to the sample surface, which deflects the laser beam. The beam's deflection corresponds to the slope of this gradient, which in turn depends on the number of photons absorbed by the film [8]. We assume that all the incident light is absorbed and none reflected. To calibrate the PDS, a flat black reference sample is which is assumed to have an absorbance $[1-\exp(-\alpha d)]$ of unity at all wavelengths. Dividing the deflection signal by the measured light intensity (number of incident photons) and by this reference sample deflection gives us the film absorbance [9].

PDS also measures all transitions, not just ones that put electrons into the conducting states. PDS can also be used without having to attach any contacts to the film. The main drawback of PDS is that for thin samples, surface defect states dominate the effective density of the material [9]. For such samples the absorption measured by PDS will be anomalously large compared with the true absorption of the bulk material.

In order to obtain the absorption coefficient from energies of ~1 eV to over 2 eV, the data from these two techniques must be combined.

B.3 DARK CONDUCTIVITY

The conductivity (σ) of a material is defined by

$$J = \sigma E \qquad \text{(B.16)}$$

where J is the current density in A/cm^2 and E is the driving electric field in V/cm. This is both a measure of the number of charge carriers and their mobility. In crystalline semiconductors, a measurement of the conductivity as a function of the temperature, below room temperature, usually has an exponential form given by

$$\sigma = \sigma_o e^{-\frac{E_{act}}{kT}} \qquad \text{(B.17)}$$

which describes thermally activated behavior. The impurities with the charge carriers reside below the conduction band of the semiconductor and thermal emission results in these carriers being excited into the conduction band giving rise to the conductivity of the material. Although amorphous semiconductors have many localized states, they are filled at room temperature and the amorphous semiconductors exhibit similar behavior to the crystalline materials. At low temperatures, however, other behavior like nearest neighbor and variable range hopping conduction, can be seen where the amorphous nature of the material is clearly demonstrated. The conductivity of amorphous semiconductors is significantly smaller than that of crystalline semiconductors. The lower conductivity can occur due to several reasons. Many of the thermally-activated carriers are not excited into extended states, but into states of the conduction or valence band states since these states are closest energetically to the dopants or the Fermi level (Fig. B.1). Furthermore, for doped materials, *a*-Si has a much lower doping efficiency and therefore a lower conductivity than c-Si. This occurs, as many of the dopant atoms are not located in four-fold coordinated sites, but in three-fold ones, where they are electronically inactive (i.e. they neither donate nor accept electrons) [10].

The dark conductivity measurement is performed by thermally evaporating coplanar aluminum contacts 7.5 mm long with gap of 0.5 mm onto the thin film to be measured. Gold wires are attached by silver epoxy. The apparatus is described elsewhere. Because the conductivity of *a*-Si:H, even doped, is so low, the contact resistance of the sample is negligible compared to its bulk resistance. The two-point contact measurement requires a uniform sample thickness of a known geometry, and assumes that conduction takes place uniformly throughout the sample. For this particular geometry, we can rewrite equation (B.16) as

$$J = \frac{I}{A} = \frac{I}{d * 7.5mm} = \sigma E = \sigma \frac{V}{0.5mm} \qquad \text{(B.18)}$$

where A is the cross-sectional area (film thickness times width of the electrodes) through which the current flows and 0.5 mm is the gap between the electrodes across which the voltage is dropped. Thus

$$\sigma = \frac{0.5mm}{7.5mm} * \frac{I}{V} * \frac{1}{d} \qquad \text{(B.19)}$$

where d is the film thickness. The samples were placed in a small vacuum chamber where they were first heated to 117 °C (removes water vapor which can lead to erroneous data [9]) and then cooled to room temperature in steps of ~10 °C while the conductivity was measured. A straight line was fit to the logarithmic plot of σ vs. 1/kT to obtain the activation energy of the material's conductivity.

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Appendix C

PUBLICATIONS AND PRESENTATIONS RESULTING FROM THIS THESIS

C.1 PUBLICATIONS

1) K. Pangal, J. C. Sturm, and S. Wagner, "Integrated amorphous and polycrystalline silicon transistors on same substrate", submitted to *IEEE Transactions on Electron Devices.*

2) K. Pangal, J. C. Sturm, S. Wagner, and N. Yao, "Thin-film transistors in polycrystalline silicon by blanket and local source/drain hydrogen plasma-seeded crystallization", submitted to *IEEE Transactions on Electron Devices.*

3) K. Pangal, J. C. Sturm, and S. Wagner, "Integration of amorphous and polycrystalline silicon thin-film transistors through selective crystallization of amorphous silicon", to be published in *Applied Physics Letters* vol. 75, 1999.

4) M. Wu, K. Pangal, J. C. Sturm, and S. Wagner, "High electron mobility polycrystalline silicon thin-film transistors on steel foil substrates", to be published in *Applied Physics Letters* vol. 75, 1999.

5) K. Pangal, Y. Chen, J. C. Sturm, S. Wagner, "Integrated amorphous and polycrystalline silicon TFTs with a single silicon layer", to be published in *Materials Research Society Symposium Proceedings* vol. 557, 1999.

6) L. Montès, L. Tsebeskov, P. M. Fauchet, K. Pangal, J. C. Sturm, S. Wagner, "Optical analysis of plasma enhanced crystallization of amorphous silicon films", *Materials Research Society Symposium Proceedings* vol. 536, pp. 505-510, 1999.

7) K. Pangal, J. C. Sturm, S. Wagner, and T. H. Buyuklimanli, "Hydrogen plasma-enhanced crystallization of hydrogenated amorphous silicon films", *Journal of Applied Physics* vol. 85, pp. 1900-1906, 1999.

8) K. Pangal, J. C. Sturm, and S. Wagner, "Hydrogen plasma-enhanced crystallization of amorphous silicon for low-temperature polycrystalline silicon TFTs", *Technical Digest of International Electron Devices Meeting*, pp. 261-264, 1998.

9) K. Pangal, J. C. Sturm, S. Wagner, "Effect of plasma treatment on crystallization behavior of amorphous silicon films", *Materials Research Society Symposium Proceedings* vol. 507, pp. 577-582, 1998.

10) K. Pangal and J. C. Sturm, "Correlation of plasma-induced charging voltage measured in-situ by microelectromechanical sensors with device degradation", *Proceedings of 2nd International Symposium on Plasma Process-Induced Damage*, pp. 203-206, 1997.

11) K. Pangal, S. L. Firebaugh, and J. C. Sturm, "Noninvasive measurement of charging in plasmas using microelectromechanical charge sensing devices", *Applied Physics Letters* vol. 69, pp. 1471-1473, 1996.

C.2 CONFERENCE PRESENTATIONS

1) K. Pangal, Y. Chen, J.C. Sturm and S. Wagner, "Integrated amorphous and polycrystalline silicon TFTs with a single silicon layer", Materials Research Society Spring Meeting, San Francisco, CA, April 1999.

2) K. Pangal, J.C. Sturm and S. Wagner, "Hydrogen-plasma-enhanced crystallization of amorphous silicon for low-temperature polycrystalline silicon TFTs", IEEE International Electron Devices Meeting, San Francisco, CA, December 1998.

Montès, L. Tsebeskov, P. M. Fauchet, K. Pangal, J. C. Sturm, S. Wagner, "Optical analysis of plasma enhanced crystallization of amorphous silicon films", Materials Research Society Fall Meeting, Boston, MA, November 1998.

4) K. Pangal, J.C. Sturm and S. Wagner, "Effect of plasma treatment on crystallization behavior of amorphous silicon films", Materials Research Society Spring Meeting, San Francisco, CA, April 1998.

5) K. Pangal and J.C Sturm, "Correlation of plasma-induced charging voltage measured in-situ by microelectromechanical sensors with device degradation", Plasma Process Induced Damage Conference, Monterey, CA, May 1997

Pangal, S. L. Firebaugh, J.C. Sturm, "Microelectromechanical charge sensing devices", IEEE Device Research Conference, Santa Barbara, CA, June 1996.